TECHNICAL MANUAL

OPERATOR'S, ORGANIZATIONAL, DIRECT SUPPORT, GENERAL SUPPORT, AND DEPOT MAINTENANCE MANUAL FOR

INTERCEPT GROUP COUNTERMEASURES RECEIVING SET AN/FLR-9(V7)/(V8)

F & M SYSTEMS CO.

HEADQUARTERS, DEPARTMENT OF THE ARMY

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SECTION I

DESCRIPTION

1-1. Scope of Manual.

This two volume manual contains installation operation, theory of operation, maintenance, and depot inspection standards for the Intercept Group AN/FLR-9(V7) and (V8) and newly designed equipments contained therein. The two configurations, AN/FLR-9(V7) and AN/FLR-9(V8), differ only in the number of equipments used. These equipments include Selector, Beam SA-1870/FLR-9(V) (bsu/biu); Selector, Beam SA-1871/FLR-9(V) (special project bsu/biu); the substation (3300-44019); and the position scanner (3300-46030). Each of these equipments is described in detail within the manual. Unless otherwise specified, descriptions of the bsu/biu also apply to the special project bsu/biu. In addition, a power supply common to each equipment is described. Publications describing support equipments used in the intercept group are listed in paragraph 1-10. Volume 1 contains maintenance description, volume 2 contains parts and wire lists.

1-2. Purpose of Manual. (See figure 1-1.)

This manual describes the Intercept Group associated with Countermeasures Receiving Set AN/FLR-9(V7)/(V8). The manual covers installation, operation, theory of operation maintenance, and depot inspection standards. Maintenance includes cleaning, inspecting, parts replacement, troubleshooting, alignment and repair for the operation and unit repairman. Depot inspection standards include a list of test equipment, tools, and special appliances required to perform associated optimum performance standards tests.

1-3. Description and Purpose.

a. Description.

1. Bsu/biu. The intercept group bsu/biu provides each mission operator with the capability of selecting any 1 of 20 antenna beams for each of 2 associated receivers at the V7 site and 20 beams for both receivers at the V8 site. Selected antenna beams provided rf signals to the receivers on one of three bands (2 MHz to 6 MHz, 6 MHz to 18 MHz, 18 MHz to 30 MHz) In selected azimuthal direction. The band and azimuth selected for each receiver is displayed at the user operator position bsu/biu.

2. Special Project Bsu/Biu. The intercept group special project bsu/biu provides certain operators with the capability of selecting all possible antenna azimuth angles, types of beams, and frequency band for a single receiver. The special project bsu/biu indicates the selected band, beam, and azimuth when the connections have been made.

3. Substation. Each intercept group substation provides interface between each bsu/biu and the position scanner. This interface amounts to line impedance matching and driving.

4. Position Scanner. The intercept group position scanner provides control and data to all bsu/biu and special project bsu/biu, as supplied by the system

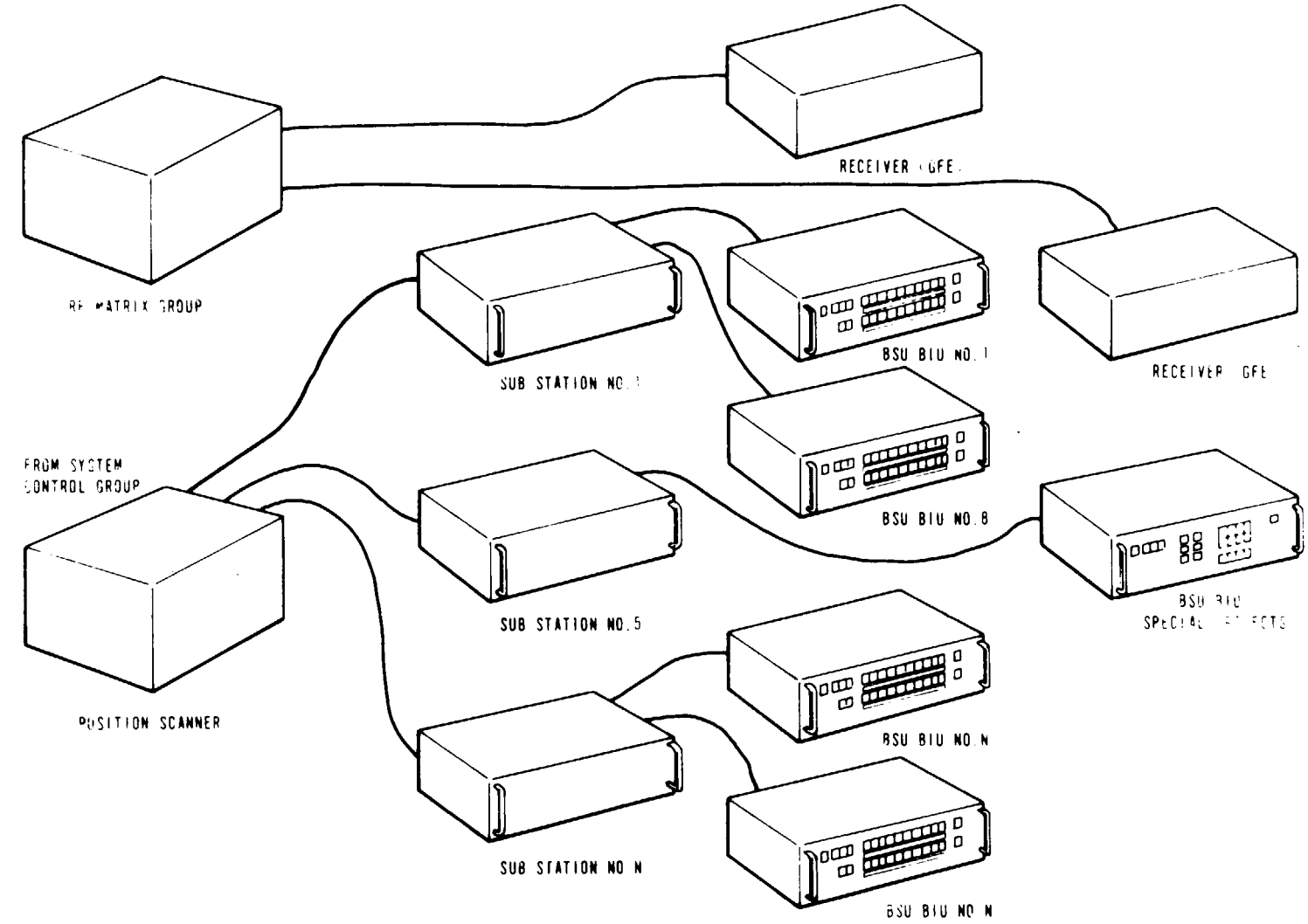


Figure 1-1. Intercept Group

control group. This interfacing includes timing, data and address recognition, and service request recognition.

b. Purpose.

1. Intercept group equipment consists of a bsu/biu at each mission operator position. The mission operator selects pre-programmed antenna beams by momentarily pressing 1 of the 20 BEAM SELECT switches and 1 of 2 receiver switches on the bsu/ biu. The antenna beam request calls up a computer program routine in the system control group computer which identifies the azimuth and rf band associated with the BEAM SELECT switch. Switchpoint closure signals are provided for the switch matrix to select the requested rf signal. The rf signal is coupled directly to the selected receiver while a switch closure verification signal is supplied to the system control group computer. This signal is converted to a BCD signal and returned to the bsu/biu as the azimuth and rf band signal. These signals provide a visual readout of the azimuth and band in use. The special project bsu/biu purpose is the same except that all beam azimuth angles are available.

2. Interface between the bsu/biu and the system control group is provided by a substation and the position scanner. The substation provides signal distribution which allows eight bsu/biu to interface with the position scanner on one input/output line. The position scanner provides proper interface to the computer.

1-4. Leading Particulars. (See table 1-1.)

Leading particulars are listed in table 1-1.

Table 1-1. Leading Particulars

Item	Power Requirements	Dimensions in Inches			Weight (lb)
		Height	Width	Depth	
Selector, Beam SA-1870 FLR-9(V) (Bsu/biu)	120 ±12 volts 47 to 63 Hz single-phase 0.5 ampere	5.2	19	13.5	18
Selector, Beam SA-1871 FLR-9(V)(Special Project bsu/biu)	120 ± 12 volts 47 to 63 Hz single-phase 0.5 ampere	5.2	19	13.5	19
Substation 3300-44019-1	120 ± 12 volts 47 to 63 Hz single-phase 0.5 ampere	5.2	9	13.5	7
Position Scanner 3300-46030-1	5 volts dc 20 amperes	28	19	6	12

1-5. Capabilities and Limitations. (See table 1-2.)

Capabilities and limitations are listed in table 1-2.

Table 1-2. Capabilities and Limitations

Characteristic	Limits
Signal Level (All Units) Positive logic used throughout Binary levels High Low	+5 volts dc +5 volts dc 0 volt dc
Operating Environment (All Units) Temperature Humidity	 0°C to 50°C Up to 95 percent relative, without condensation
Output signal of bsu/biu Bsu/biu Special project bsu/biu	 7-bit serial word to input of position scanner 14-bit serial word to input of position scanner
Input signal to (either) bsu/biu	14-bit receiver beam assignment word from computer via position scanner 9-bit address word from position scanner

1-6. Equipment Supplied. (See table 1-3.)

Equipment supplied is listed in table 1-3.

Table 1-3. Equipment Supplied

Item	Name	Quantity	
		AN/FLR-9(V7)	AN/FLR-9(V8)
1	Selector, Beam SA-1870/FLR-9(V) (bsu/biu)	133	316
2	Substation 3300-44019-1	19	42
3	Selector, Beam SA-1871/FLR-9(V) (special project bsu/biu)	3	3

Table 1-3. Equipment Supplied (Continued)

Item	Name	Quantity	
		AN/FLR-9(V7)	AN/FLR-9(V8)
4	Position Scanner 3300-46030-1	1	1
5	Connector, Rf Attenuator 3300-40025-1	One for each receiver	

1-7. Equipment Required But Not Supplied. (See table 1-4.)

Equipment required but not supplied with the intercept group is listed in table 1-4.

Table 1-4. Equipment Required But Not Supplied

Item	Name	Quantity
1	Radio Receiver R-390A/URR or equivalent (GFE)	Two for each bsu/biu
2	Radio Receiver R-390A/URR or equivalent (GFE)	One for each special project bsu/biu

1-8. Model Differences.

Equipments used in the AN/FLR-9(V7)and (V8) Intercept Groups are identical. The only difference in the two groups is the number of equipments used and the configuration of the SOM Console at V8(see fig 2-1a). For quantity, refer to table 1-3.

1-9. Reference Designation. (See tables 1-5 and 1-6 and figure 1-2.)

One position scanner is used in the intercept group. This unit is located in rack 209 with the system control group equipment. Three special project bsu/biu are used in the AN/FLR-9(V7) and (V8) sites. At the AN/FLR-9(V8) site, 317 bsu/biu are supplied whereas 134 are supplied in the AN/FLR-9(V7) site. In the AN/FLR-9(V8) site, 43 substations are supplied, and 20 are supplied at the AN/FLR-9(V7) site. The preceding units, with the exception of the position scanner, are located at positions determined by the user. The unit locations are listed in tables 1-5 and 1-6 and are typical locations for these units. As many as eight bsu/biu are listed with a substation which is associated with these units. The listing consists of two columns, Row and Rack. The letter U in the Rack column indicates the upper unit, letter L indicates lower unit. Figure 1-2 illustrates a typical row of equipment.

Table 1-5. AN/FLR-9(V7) Reference Designators and Bsu/Biu Address

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
0	000	1	01	20	01	01	01	01U
		2					01	01L
1	001	1	01	20	01	03	01	03U
		2					01	03L
2	002	1	01	20	01	07	01	07U
		2					01	07L
3	003	1	01	20	01	08	01	10U
		2					01	10L
4	004	1		N/A*				
		2						
5	005	1	01	20	01	12	01	12U
		2					01	12L
6	006	1	01	20	01	13	01	15U
		2					01	15L
7	007	1	01	20	01	17	01	17U
		2					01	17L
8	008	1	01	20	01	20	01	20U
		2					01	20L
9	009	1		N/A				
		2						
10	00A	1	02	18	02	01	02	01U
		2					02	01L
11	00B	1	02	18	02	03	02	05U
		2					02	05L
12	00C	1	02	18	02	06	02	06U
		2					02	06L
13	00D	1	02	18	02	08	02	10U
		2					02	10L
14	00E	1		N/A				
		2						
15	00F	1	02	18	02	11	02	11U
		2					02	11L
16	010	1	02	18	02	15	02	13U
		2					02	14L
17	011	1	02	18	02	16U	02	16U
		2					02	16L
18	012	1	03	20	03	01	03	01U
		2					03	01L
19	013	1		N/A				
		2						
20	014	1	03	20	03	03	03	03U
		2					03	03L

*N/A defines not assigned units.

Table 1-5. AN/FLR-9(V7) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
21	015	1	03	20	03	07	03	07U
		2					03	07L
22	016	1	03	20	03	08	03	10U
		2					03	10L
23	017	1	03	20	03	12	03	12U
		2					03	12L
24	018	1		N/A				
		2						
25	019	1	03	20	03	13	03	15U
		2					03	15L
26	01A	1	03	20	03	17	03	17U
		2					03	18L
27	01B	1	03	20	03	20	03	20U
		2					03	20L
28	01C	1	04	18	04	o1	04	01U
		2						01L
29	01D	1		N/A				
		2						
30	01E	1	04	18	04	05	04	03U
		2					04	03L
31	01F	1	04	18	04	06	04	06U
		2					04	06L
32	020	1	04	18	04	10	04	08U
		2					04	08L
33	021	1	04	18	04	11	04	11U
		2					04	11U
34	022	1		N/A				
		2						
35	023	1	04	18	04	15	04	13U
		2					04	13L
36	024	1	04	18	04	18	04	16U
		2					04	16L
37	025	1	05	20	05	01	05	01U
		2					05	01L
38	026	1	05	20	05	03	05	03U
		2					05	03L
39	027	1		N/A				
		2						
40	028	1	05	20	05	07	05	07U
		2					05	10L
41	029	1	05	20	05	08	05	10U
		2					05	10L

Table 1-5. AN/FLR-9(V7) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
2	02A	1	05	20	05	12	05	12U
		2					05	12L
43	02B	1	05	20	05	13	05	15U
		2					05	15L
44	02C	1		N/A				
		2						
45	02D	1	05	20	05	17	05	17U
		2					05	17L
46	02E	1	05	20	05	20	05	20U
		2					05	20L
47	02F	1	06	18	06	01	06	01U
		2					06	01L
48	030	1	06	18	06	05	06	03U
		2					06	03L
49	031	1		N/A				
		2						
50	032	1	06	18	06	06	06	06U
		2					06	06L
51	033	1	06	18	06	10	06	08U
		2					06	08L
52	034	1	06	20	06	11	06	11U
		2					06	11L
53	035	1	06	18	06	15	06	13U
		2						13L
54	036	1		N/A				
		2						
55	037	1	06	18	06	18	06	16U
		2					06	16L
56	038	1	07	18	07	01	07	01U
		2					07	01L
57	039	1	07	18	07	05	07	03U
		2					07	03L
58	03A	1	07	18	07	06	07	06U
		2					07	06L
59	03B	1		N/A				
		2						
60	03C	1	07	18	07	10	07	08U
		2					07	08L
61	03D	1	07	18	07	11	07	11U
		2					07	11L
62	03E	1	07	18	07	15	07	13U
		2					07	13L

Table 1-5. AN/FLR-9(V7) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
63	03F	1	07	18	07	18	07	16U
		2					07	16L
64	040	1 }		N/A				
		2 }						
65	041	1	08	20	08	01	08	01U
		2					08	01L
66	042	1	08	20	08	05	08	03U
		2				2	08	03L
67	043	1	08	20	08	06	08	06U
		2					08	06L
68	044	1	08	20	08	10	08	08U
		2					08	08L
69	045	1 }		N/A				
		2 }						
70	046	1	08	20	08	11	08	11U
		2					08	11L
71	047	1	08	20	08	15	08	13U
		2					08	13L
72	048	1	08	20	08	16	08	16U
		2					08	16L
73	049	1	08	20	08	20	08	18U
		2					08	18L
74	04A	1 }		N/A				
		2 }						
75	04B	1	09	18	09	01	09	01U
		2					09	01L
76	04C	1	09	18	09	05	09	03U
		2					09	03L
77	04D	1	09	18	09	06	09	06U
		2					09	06L
78	04E	1	09	18	09	10	09	08u
		2					09	08L
79	04F	1 }		N/A				
		2 }						
80	050	1	09	18	09	11	09	11U
		2					09	11L
81	051	1	09	18	09	15	09	13U
		2					09	13L
82	052	1	09	18	09	18	09	16U
		2					09	16L
83	053	1	10	20	10	01	10	01U
		2					10	01L

Table 1-5. AN/FLR-9(v7) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
84	054	1 2		N/A				
85	055	1	10	20	10	05	10 10	03U 03L
86	056	1 2	10	20	10	06	10 10	06U 06L
87	057	1 2	10	20	10	10	10 10	08U 08L
88	058	1 2	10	20	10	11	10 10	11U 11L
89	059	1 2		N/A				
90	05A	1 2	10	20	10	15	10 10	13U 13L
91	058	1 2	20	N/A	10	16	10 10	16U 16L
92	05C	1 2	10	20	10	20	10 10	18U 18L
93	05D	1 2	11	18	11	01	11	01U
94	05E	1 2		N/A				
95	05F	1 1	11	18	11	05	11 11	03U 03L
96	060	2	11	18	11	06	11 11	06u 06L
97	061	1 2	11	18	11	10	11 11	08U 08L
98	062	1 2	11	18	11	11	11 11	11U 11L
99	063	1 2		N/A				
100	064	1 2	11	18	11	15	11 11	13U 13L
101	065	1 2	11	18	11	18	11 11	16u 16L
102	066	1 2	12	20	12	01	12 12	01U 01L
103	067	1 2	12	20	12	05	12 12	03U 03L
104	068	1 2		N/A				

Table 1-5. AN/FLR-9(V7) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
105	069	1	12	20	12	06	12	06U
		2					12	06L
106	06A	1	12	20	12	10	12	08U
		2					12	08L
107	06B	1	12	20	12	11	12	11U
		2					12	11L
108	06C	1	12	20	12	15	12	13U
		2					12	13L
109	06D	1		N/A				
		2						
110	06E	1	12	20	11	19	11	19U
		2					11	19L
111	06F	1	12	20	12	20	12	18U
		2					12	18L
112	070	1	15	09	13	04	13	04
		2					N/A	N/A
113	071	1	15	09	13	05	13	05
		2					N/A	N/A
114	072	1		N/A				
		2						
115	073	1	15	09	14	03	14	04
		2					N/A	N/A
116	074	1	15	09	15	03	15	03U
		2					15	03L
117	075	1	15	09	15	04	15	04U
		2					15	04L
118	076	1	15	09	15	08	15	08U
		2					15	08L
119	077	1		N/A				
		2						
120	078	1	15	09	15	09	15	09U
		2					15	09L
121	079	1	N/A	N/A	N/A	N/A	16	04
		2	N/A	N/A				
122	07A	1	N/A	N/A	N/A	N/A	16	06U
		2					16	06L
123	078	1	N/A	N/A	N/A	N/A	16	07U
		2	N/A	N/A				
124	07C	1		N/A				
		2						
125	07D	1	N/A	N/A	N/A	N/A	16	11U
		2					N/A	N/A

Table 1-5. AN/FLR-9(V7) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
126	07E	1	N/A	N/A	N/A	N/A	17	01
		2					N/A	N/A
127	07F	1	N/A	N/A	N/A	N/A	17	02
		2					N/A	N/A
128	080	1	N/A	N/A	N/A	N/A	17	06U
		2					17	06L
129	081	1			N/A			
		2						
130	082	1	N/A	N/A	N/A	N/A	17	12
		2					N/A	N/A
131	083	1	N/A	N/A	18	01	18	01U
		2					18	01L
132	084	1	N/A	N/A	18	04	18	06U
		2					18	06L
133	085	1	18	13	18	07	18	09U
		2					18	09L
134	086	1			N/A			
		2						
135	087	1	18	13	18	10	18	12U
		2					18	12L
136	088	1	18	13	18	13	18	15U
		2					18	15L
137	089	1	18	13	19	0I	19	03U
		2					19	03L
138	08A	1	19	13	19	04	19	06U
		2					19	06L
139	08B	1			N/A			
		2						
140	08C	1	19	13	19	19	07	19U
		2					19	09L
141	08D	1	19	13	19	10	19	12U
		2					19	12L
142	08E	1	19	13	19	13	19	15U
		2					19	15L
143	08F	1	19	13	20	01	20	03U
		2					20	03L
144	090	1			N/A			
		2						
145	091	1	21	13	20	04	20	06U
		2					20	06L
146	092	1	21	13	20	07	20	09U
		2					20	09L

Table 1-5. AN/FLR-9(V7) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
147	093	1	21	13	20	10	20	12U
		2					20	12L
148	094	1	19	13	20	13	20	15U
		2						15L
149	095	1 }	N/A					
		2 }						
150	096	1	19	13	21	01	21	03U
		2					21	03L
151	097	1	21	13	21	04	21	06U
		2					21	06L
152	098	1	21	13	21	07	21	09U
		2					21	09L
153	099	1	21	13	21	10	21	12U
		2					21	12L
154	09A	1 }	N/A					
		2 }						
155	09B	1	21	13	21	13	21	15U
		2					21	15L
156	09C	1	21	13	22	01	22	01U
		2					22	01L
157	09D	1	22	13	22	04	22	06U
		2					22	06L
158	09E	1	22	13	22	07	22	09U
		2					22	09L
159	09F	1 }	N/A					
		2 }						
160	0A0	1	22	13	22	10	22	12U
		2					22	12L
161	0A1	1	22	13	22	13	22	15U
		2					22	15L
162	0A2	1	22	13	23	01	23	03U
		2					23	03L
163	0A3	1	22	13	23	04	23	06U
		2					23	06L
164	0A4	1 }	N/A					
		2 }						
165	0A5	1	22	13	23	07	23	09U
		2					23	09L
166	0A6	1	22	13	23	12	23	12U
		2					23	12L
167	0A7	1	24	02	23	13	23	15U
		2					23	12L

Table 1-5. AN/FLR-9(V7) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	**Hex**		**Row**	**Rack**	**Row**	**Rack**	**Row**	**Rack**
168	0A8	1	24	02	24	02	24	02
		2					24	03
169	0A9	1 }	N/A					
		2 }						
170	0AA	1	24	02	25	01	25	11
		2					25	02
171	0AB	1	24	02	25	04	25	04
		2					25	05
172	0AC	1	24	02	25	07	25	07
		2					25	08
173	0AD	1 }	N/A					
		2 }						
496	IF0	*	Flash Pos 1		Flash Pos 1		Flash Pos 1	
498	IF2	*	Flash Pos 1		Flash Pos 2		Flash Pos 2	
500	IF4	*			Flash Pos 3		Flash Pos 3	

* Only 1 receiver is associated with bsu/biu address 496, 498, and 500.

Table 1-6. AN/FLR 9(V8) Reference Designators and Bsu/Biu Address

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	**Hex**		**Row**	**Rack**	**Row**	**Rack**	**Row**	**Rack**
0	000	1	30	14	30	14	30	12U
		2					30	12L
1	001	1	30	14	30	15	30	13U
		2					30	13L
2	002	1	30	14	30	13	30	16U
		2					30	16L
3	003	1	30	14	30	16	30	17U
		2					30	17L
4	004	1	30	14	31	11	31	17U
		2					31	11L
5	005	Test	Loc. 217A7		Loc. 217A6		Loc. 217A5	
6	006	1	30	14	31	21	31	21U
		2					31	21L
7	007	1	30	14	31	22	31	22U
		2					31	22L
8	008	1	33	10	32	01	32	01U
		2					32	01L

Table 1-6. AN/FLR 9(V8) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
9	009	1	33	10	32	05	32	03U
		2					32	03L
10	00A	1	33	10	32	06	32	06U
		2					32	06L
11	00B	1	33	10	32	10	32	08U
		2					32	08L
12	00C	1	33	10	32	11	32	11U
		2					32	11L
13	00D	1	33	10	32	15	32	13U
		2					32	13L
14	00E	1	33	02	33	01	33	01U
		2					33	01L
15	00F	1	33	02	33	05	33	03U
		2					33	03L
16	010	1	33	02	33	06	33	06U
		2					33	06L
17	011	1	33	10	33	10	33	08U
		2					33	08L
18	012	1	33	10	33	13	33	11U
		2					33	11L
19	013	1	37	02	34	01	34	01U
		2					34	01L
20	014	1	34	13	34	05	34	03U
		2					34	03L
21	015	1	34	13	34	06	34	06U
		2					34	06L
22	016	1	34	13	34	10	34	08u
		2					34	08L
23	017	1	34	13	34	11	34	11U
		2					34	11L
24	018	1	34	13	34	15	34	13U
		2					34	13L
25	019	1	34	13	34	16	34	16U
		2					34	16L
26	01A	1	34	13	34	20	34	18U
		2					34	18L
27	018	1	34	13	34	23	34	21U
		2					34	21L
28	01C	1	37	02	35	01	35	01U
2							35	01L
29	01D	1	35	13	35	05	35	03U
		2					35	03L
30	01E	1	35	13	35	06	35	06U
		2					35	06L

Table 1-6. AN/FLR 9(V8) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
31	01F	1	35	13	35	10	35	08U
		2					35	08L
32	020	1	35	13	35	11	35	11U
		2					35	11L
33	021	1	35	13	35	15	35	13U
		2					35	131
34	022	1	35	13	35	16	35	16U
		2					35	16L
35	023	1	35	13	35	20	35	18U
		2					35	18L
36	024	1	35	13	35	23	35	21U
		2					35	21L
37	025	1	37	02	36	01	36	01U
		2					36	01L
38	026	1	36	13	36	05	36	03U
		2					36	03L
39	027	1	36	13	36	06	36	06U
		2	36					06L
40	028	1	36	13	36	10	36	08U
		2					36	08L
41	029	1	36	13	36	10	36	11U
		2					36	11L
42	02A	1	36	13	36	15	36	13U
		2					36	13L
43	02B	1	36	13	36	16	36	16U
		2					36	16L
44	02C	1	36	13	36	20	36	18U
		2					36	18L
45	02D	1	36	13	36	23	36	21U
		2					36	21L
46	02E	1	37	02	37	01	37	01U
		2					37	01L
47	02F	1	37	13	37	05	37	03U
		2					37	03L
48	030	1	37	13	37	06	37	06U
		2					37	06L
49	031	1	37	13	37	10	37	08U
		2					37	08L
50	032	1	37	13	37	11	37	11U
		2					37	11L
51	033	1	37	13	37	15	37	13U
		2					37	13L
52	034	1	37	13	37	16	37	16U
		2					37	16L

Table 1-6. AN/FLR 9(V8) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
53	035	1	37	13	37	20	37	18U
		2					37	18L
54	036	1	37	13	37	23	37	21U
		2					37	21L
55	037	1	37	02	38	01	38	01U
		2					38	01L
56	038	1	38	13	38	05	38	03U
		2					38	03L
57	039	1	38	13	38	06	38	06U
		2					38	06L
58	03A	1	38	13	38	10	38	08u
		2					38	08L
59	03B	1	39	13	38	11	38	11U
		2					38	11L
60	03C	1	38	13	38	15	38	13U
		2					38	13L
61	03D	1	38	13	38	16	38	16U
		2					38	16L
62	03E	1	38	13	38	20	38	18U
		2					38	18L
63	03F	1	38	13	38	23	38	21U
		2					38	21L
64	040	1	37	02	39	01	39	01U
		2					39	01L
65	041	1	39	13	39	05	39	03U
		2					39	03L
66	042	1	39	13	39	06	39	06U
		2					39	06L
67	043	1	39	13	39	10	39	08u
		2					39	08L
68	044	1	39	13	39	11	39	11U
2							39	11L
69	045	1	39	13	39	15	39	13U
		2					39	13L
70	046	1	39	13	39	16	39	16U
2							39	16L
71	047	1	39	13	39	20	39	18U
		2					39	18L
72	048	1	39	13	39	23	39	21U
		2					39	21L
73	049	1	37	02	40	01	40	01U
		N/A						
74	04A	1	41	01	41	01	41	01U
		2					41	01L

Table 1-6. AN/FLR 9(V8) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
75	04B	1	41	01	41	02	41	02U
		2					41	02L
76	04C	1	41	01	41	06	41	6U
		2					41	06L
77	04D	1	41	01	41	07	41	07U
		2					41	07L
78	04E	1	41	01	41	11	41	11U
			2				41	11L
79	04F	1	41	01	41	12	41	12U
		2				41	12L	
80	050	1	41	01	41	16	41	16U
		2					41	16L
81	051	1	41	0l	41	17	41	17U
		2					41	17L
82	052	1	50	23	50	05	50	05
		N/A						
83	053	1	50	23	50	14	50	14U
		2					50	14L
84	054	1	50	23	50	17	50	17U
		2					50	17L
85	055	1	50	23	50	20	50	20U
		2				50	20L	
86	056	1	50	23	50	23	50	23U
		2				50	23L	
87	057	1	50	23	50	26	50	26U
		2				50	26L	
88	058	1	50	23	51	19	51	19U
		2					51	19L
89	059	1	50	23	51	22	51	22U
		2					51	22L
90	05A	1	33	02	51	25	51	25U
		2					51	25L
91	05B	1	33	02	51	28	51	28U
		2					51	28L
92	05C							
93	05D							
94	05E	Not Used						
95	05F							
96	060	.						

Table 1-6. AN/FLR 9(V8) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
97	061	Not Used						
98	062							
99	063							
100	064							
101	065	1	01	20	01	5L	01	03U
2					01		01	03L
102	066	1	01	20	01	5U	01	04U
		2			01		01	
103	067	1	01	20	01	10L	01	
		2			01		01	
104	068	1	01	20	01	10L	01	09U
		2			01		01	09L
105	069	1	01	20	01	15L	01	13U
		2			01		01	13L
106	06A	1	01	20	01	15U	01	14U
		2			01		01	14L
107	06B	1	01	20	01	20L	01	18U
		2			01		01	18L
108	06C	1	01	20	01	20U	01	19U
		2			01		01	19L
109	06D	1	01	39	01	25L	01	23U
		2			01		01	23L
110	06E	1	01	39	0l	25U	01	24U
		2			01		01	24L
111	06F	1	01	39	01	30L	01	28U
		2			01		01	28L
112	070	1	01	39	01	30U	01	29U
		2			01		01	29L
113	071	1	01	39	01	39	01	41
		2			01	42	01	42
114	072	1	02	20	02	05L	02	03U
		2			02		02	03L
115	073	1	02	20	02	05U	02	04U
		2			02		02	04L
116	074	1	02	20	02	10L	02	08U
		2			02		02	08L
117	075	1	02	20	02	10L	02	09L
		2			02		02	09L
118	076	1	02	20	02	15L	02	13U
		2			02		02	13L

Table 1-6. AN/FLR 9(V8) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
119	077	1	02	20	02	15U	02	14U
		2					02	14L
120	078	1	02	20	02	20L	02	18U
		2					02	18L
121	079	1	02	20	02	20U	02	19U
		2					02	19L
122	07A	1	02	30	02	25L	02	23U
		2					02	23L
123	07B	1	02	30	02	25U	02	24U
		2					02	24L
124	07C	1	02	30	02	30U	02	28U
		2					02	28L
125	07D	1	02	30	02	30L	02	29U
		2					02	29L
126	07E	1	03	20	03	05U	03	03U
		2					03	03L
127	07F	1	03	20	03	05L	03	04U
		2					03	04L
128	080	1	03	20	03	10U	03	08U
		2					03	08L
129	081	1	03	20	03	10L	03	09U
		2					03	09L
130	082	1	03	20	03	15U	03	13U
		2					03	13L
131	083	1	03	20	03	15L	03	14U
		2					03	14L
132	084	1	03	20	03	20U	03	18U
		2					03	18L
133	085	1	03	20	03	20L	03	19U
		2					03	19L
134	086	1	02	30	03	25U	03	23U
		2					03	23L
135	087	1	02	30	03	25L	03	24U
		2					03	24L
136	088	1	02	30	03	30U	03	28U
							03	28L
137	089	21	02	30	03	30L	03	29U
		2					03	29L
138	08A	1	01	39	03	39	03	41
		2					03	42
139	08B	1	04	20	04	05U	04	03U
		2					04	03L
140	08C	1	04	20	04	05L	04	04U
		2					04	04L

Table 1-6. AN/FLR 9(V8) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
141	08D	1	04	20	04	10U	04	08U
		2					04	08L
142	08E	1	04	20	04	10L	04	09U
		2					04	09L
143	08F	1	04	20	04	15U	04	13U
		2					04	13L
144	090	1	04	20	04	15L	04	14U
		2					04	14L
145	091	1	04	20	04	20U	04	18U
		2					04	18L
146	092	1	04	20	04	20L	04	19U
		2					04	19L
147	093	1	04	30	04	25U	04	23U
		2					04	23L
148	094	1	04	30	04	25L	04	24U
		2					04	24L
149	095	1	04	30	04	30U	04	28U
		2					04	28L
150	096	1	04	30	04	30L	04	29U
		2					04	29L
151	097	1	05	20	05	05U	05	03U
		2					05	03L
152	098	1	05	20	05	05L	05	04u
		2					05	04L
153	099	1	05	20	05	10U	05	08U
		2					05	08L
154	09A	1	05	20	05	10L	05	09U
		2					05	09L
155	09B	1	05	20	05	15U	05	13U
		2					05	13L
156	09C	1	05	20	05	15L	05	14U
		2					05	14L
157	09D	1	05	20	05	20U	05	18U
		2					05	18L
158	09E	1	05	20	05	20L	05	19U
		2					05	19L
159	09F	1	04	30	05	25U	05	23U
		2					05	23L
160	0A0	1	04	30	05	25L	05	24U
		2					05	24L
161	0A1	1	04	30	05	30U	05	28U
		2					05	28L
162	0A2	1	04	30	05	30L	05	29U
		2					05	29L

Table 1-6. AN/FLR 9(V8) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
163	0A3	1	07	37	05	39	05	41
		2					05	42
164	0A4	1	06	20	06	05U	06	03U
		2					06	03L
165	0A5	1	06	20	06	05L	06	04u
		2					06	04L
166	0A6	1	06	20	06	10U	06	08U
		2					06	08L
167	0A7	1	06	20	06	10L	06	09U
		2					06	09L
168	0A8	1	06	20	06	15U	06	13U
		2					06	13L
169	0A9	1	06	20	06	15L	06	14U
		2					06	14L
170	0AA	1	06	20	06	20U	06	18U
		2					06	18L
171	0AB	1	06	20	06	20L	06	19U
		2					06	19L
172	0AC	1	06	30	06	25U	06	23U
		2					06	23L
173	0AD	1	06	30	06	25L	06	24U
		2					06	24L
174	0AE	1	06	30	06	30U	06	28U
		2					06	28L
175	0AF	1	06	30	06	30L	06	29U
		2					06	29L
176	0B0	1	06	30	06	31	06	31U
		2					06	31L
177	0B1	1	06	30	06	32	06	32U
		2					06	32L
178	0B2	1	06	30	06	35	06	35U
		2					06	35L
179	0B3	1	06	30	06	36	06	36U
		2					06	36L
180	0B4	1	07	29	07	08U	07	06U
		2					07	06L
181	0B5	1	07	29	07	08L	07	07U
		2					07	07L
182	0B6	1	07	29	07	16U	07	14U
		2					07	14L
183	0B7	1	07	29	07	16L	07	15U
		2					07	15L
184	0B8	1	07	29	07	24U	07	22U
		2					07	22L

Table 1-6. AN/FLR 9(V8) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
185	0B9	1	07	29	07	24L	07	23U
		2					07	23L
186	OBA	1	07	29	07	29U	07	27U
		2					07	27L
187	0BB	1	07	29	07	29L	07	28U
		2					07	28L
188	0BC	1	07	37	07	37	07	39
		2					07	40
189	0BD	1	08	32	08	08U	08	06U
		2					08	06L
190	0BD	1	08	32	08	08L	08	07U
		2					08	07L
191	OBF	01	8	32	08	16U	08	14U
		2					08	14L
192	0C0	1	08	32	08	16L	08	15U
		2					08	15L
193	0C1	1	08	32	08	24U	08	22U
		2					08	22L
194	0C2	1	08	32	08	24L	08	23U
		2					08	23L
195	0C3	1	08	32	08	32U	08	30U
		2					08	30L
196	0C4	1	08	32	08	32L	08	31U
		2					08	31L
197	0C5	1	07	37	08	37U	08	35U
		2					08	35L
198	0C6	1	07	37	08	37L	08	36U
		2					08	36L
199	0C7	1	09	20	09	01	09	01U
	2						09	01L
200	0C8	1	09	20	09	05	09	03U
	2						09	03L
201	0C9	1	09	20	09	06	09	06U
	2						09	06L
202	0CA	1	09	20	09	10	09	08U
	2						09	08L
203	0CB	1	09	20	09	11	09	11U
	2						09	11L
204	0CC	1	09	20	09	15	09	13U
	2						09	13L
205	0CD	1	09	20	09	16	09	16U
	2						09	16L
206	0CE	1	09	20	09	20	09	18U
	2						09	18L

Table 1-6. AN/FLR 9(V8) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
207	0CF	1	09	38	09	21	09	21U
		2					09	21L
208	0D0	1	09	38	09	25	09	23U
		2					09	23L
209	0D1	1	09	38	09	26	09	26U
		2					09	26L
210	0D2	1	09	38	09	30	09	28U
		2					09	28L
211	0D3	1	09	38	09	31	09	31U
		2					09	31L
212	0D4	1	09	38	09	35	09	33U
		2					09	33L
213	0D5	1	09	38	09	38	09	36U
		2					09	36L
214	0D6	1	10	18	10	01	10	03U
		2					10	03L
215	0D7	1	10	18	10	04	10	06U
		2					10	06L
216	0D8	1	10	18	10	08	10	08u
		2					10	08L
217	0D9	1	10	18	10	09	10	11U
		2					10	11L
218	0DA	1	10	18	10	13	10	13U
		2					10	13L
219	0DB	1	10	18	10	14	10	16U
		2					10	16L
220	0DC	10	18	10	18		10	18U
		2					10	18L
221	0DD	1	10	38	10	19	10	21U
		2					10	21L
222	0DE	1	10	38	10	23	10	23U
		2					10	23L
223	0DF	1	10	38	10	24	10	26U
		2					10	26L
224	0E0	1	10	38	10	28	10	28U
		2					10	28L
225	0E1	1	10	38	10	29	10	31U
		2					10	31L
226	0E2	1	10	38	10	33	10	33U
		2					10	33L
227	0E3	1	10	38	10	34	10	36U
		2					10	36L
228	0E4	1	10	38	10	38	10	38U
		2					10	38L

Table 1-6. AN/FLR-9 (V8) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
229	0E5	1	11	20	11	01	11	01U
		2					11	01L
230	0E6	1	11	20	11	05	11	03U
		2					11	03L
231	0E7	1	11	20	11	06	11	06U
		2					11	06L
232	0E8	1	11	20	11	10	11	08U
		2					11	08L
233	0E9	1	11	20	11	20	11	11U
		2					11	11L
234	0EA	1	11	20	11	15	11	13U
		2					11	13L
235	0EB	1	11	20	11	20	11	16U
		2					11	16L
236	0EC	1	11	20	11	20	11	18U
		2					11	18L
237	0ED	1	11	38	11	21	11	21U
		2					11	21L
238	0EE	1	11	38	11	25	11	23U
		2					11	23L
239	0EF	1	11	38	11	26	11	26U
		2					11	26L
240	0F0	1	11	38	11	30	11	28U
		2					11	28L
241	0F1	1	11	38	11	31	11	31U
		2					11	31L
242	0F2	1	11	38	11	35	11	33U
		2					11	33L
243	0F3	1	11	38	11	38	11	36U
		2					11	36L
244	0F4	1	12	18	12	01	12	03U
		2					12	03L
245	0F5	1	12	18	12	04	12	06U
		2					12	06L
246	0F6	1	12	18	12	08	12	08U
		2					12	08L
247	0F7	1	12	18	12	09	12	11U
		2					12	11L
248	0F8	1	12	18	12	13	12	13U
		2					12	13L
249	0F9	1	12	18	12	14	12	16U
		2					12	16L
250	0FA	1	12	18	12	18	12	18U
		2					12	18L

Table 1-6. AN/FLR-9 (V8) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
251	0FB	1	12	38	12	19	12	21U
		2					12	21L
252	0FC	1	12	38	12	23	12	23U
		2					12	23L
253	0FD	1	12	38	12	24	12	26U
		2					12	26L
254	0FE	1	12	38	12	28	12	28U
		2					12	28L
255	0FF	1	12	38	12	29	12	31U
		2					12	31L
256	100	1	12	38	12	33	12	33U
		2					12	33L
257	101	1	12	38	12	34	12	36U
		2					12	36L
258	102	1	12	38	12	38	12	38U
		2					12	38L
259	103	1	13	20	13	01	13	01U
		2					13	01L
260	104	1	13	20	13	05	13	03U
		2					13	03L
261	105	1	13	20	13	06	13	06U
		2					13	06L
262	106	1	13	20	13	10	13	18U
		2					13	08L
263	107	1	13	20	13	11	13	11U
		2					13	11L
264	108	1	13	20	13	15	13	13U
		2					13	13L
265	109	1	13	20	13	16	13	16U
		2					13	16L
266	10A	1	13	20	13	20	13	18U
		2					13	18L
267	10B	1	13	38	13	21	13	21U
		2					13	21L
268	10C	1	13	38	13	25	13	23U
		2		1			13	23L
269	10D	1	13	38	13	26	13	26U
		2					13	26L
270	10E	1	13	38	13	30	13	28U
		2					13	28L
271	10F	1	13	38	13	31	13	31U
		2					13	31L
272	110	1	13	38	13	35	13	33U
		2					13	33L

Table 1-6. AN/FLR-9 (V8) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
273	111	1	13	38	13	38	13	36U
		2					13	36L
274	112	1	14	18	14	01	14	03U
		2					14	03L
275	113	1	14	18	14	04	14	06U
		2					14	06L
276	114	1	14	18	14	08	14	08U
		2					14	08L
277	115	1	14	18	14	09	14	11U
		2					14	11L
278	116	1	14	18	14	13	14	13U
		2					14	13L
279	117	1	14	18	14	14	14	16U
		2					14	16L
280	118	1	14	18	14	18	14	18U
		2					14	18L
281	119	1	14	38	14	19	14	21U
		2					14	21L
282	11A	1	14	38	14	23	14	23U
		2					14	23L
283	11B	1	14	38	14	24	14	26U
		2					14	26L
284	11C	1	14	38	14	28	14	28U
		2					14	28L
285	11D	1	14	38	14	29	14	31U
		2					14	31L
286	11E	1	14	38	14	33	14	33U
		2					14	33L
287	11F	1	14	38	38	34	14	36U
		2					14	36L
288	120	1	14	38	14	38	14	38U
		2					14	38L
289	121	1	15	01	15	01	15	01U
		2					15	01L
290	122	1	15	01	15	05	15	03U
		2					15	03L
291	123	1	15	01	15	06	15	06U
		2					15	06L
292	124	1	15	01	15	10	15	08U
		2					15	08L
293	125	1	14	18	15	13	15	11U
		2					15	11L
294	126	1	15	01	16	01	16	03U
		2					16	03L

Table 1-6. AN/FLR-9 (V8) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	Hex		Row	Rack	Row	Rack	Row	Rack
295	127	1	15	01	16	04	16	06U
		2					16	06L
296	128	1	15	01	16	07	16	09U
		2					16	09L
297	129	1	15	01	16	10	16	12U
		2					16	12L
298	12A	1	18	20	17	18	17	18U
		N/A						
299	12B	1	18	20	17	19	17	19U
		2					17	19L
300	12C	1	18	20	18	05U	18	04
		2					18	06
301	112D	1	18	20	18	16	18	15
		2					18	16
302	12E	1	18	20	18	18	18	17
		2					18	18
303	12F	1	18	20	18	20	18	19
		2					18	20
304	130	1	19	20	19	05U	19	03U
		2					19	03L
305	131	1	19	20	19	05L	19	04u
		2					19	04L
306	132	1	19	20	19	10U	19	08U
		2					19	08L
307	133	1	19	20	19	10L	19	09U
		2					19	09L
308	134	1	19	20	19	15U	19	13U
		2					19	13L
309	135	1	19	20	19	15L	19	14U
		2					19	14L
310	136	1	19	20	19	20U	19	18U
		2					19	18L
311	137	1	19	20	19	20L	19	19U
		2					19	19L
312	138	1	07	37	20	04	20	01
		2					20	02
313	139	1	20	27	20	12U	20	13U
		2					20	13L
314	13A	1	20	27	20	12L	20	14U
		2					20	14L
315	13B	1	20	27	20	17U	20	18U
		2					20	18L
316	13C	1	20	27	20	17L	20	19U
		2					20	19L

Table 1-6. AN/FLR-9 (V8) Reference Designators and Bsu/Biu Address (Continued)

Bsu/Biu Address		Receiver	Substation		Bsu/Biu		Receiver Location	
Dec	**Hex**		**Row**	**Rack**	**Row**	**Rack**	**Row**	**Rack**
317	13D	1	20	27	20	22U	20	23U
		2					20	23L
318	13E	1	20	27	20	22L	20	24U
		2					20	24L
319	13F	1	20	27	20	27U	20	28U
		2					20	28L
320	140	1	20	27	20	27L	20	29U
		2					20	29L
321	141	1	18	20	18	09	18	09U
		Not used						
349	15D	1	Output terminated at output MPP jack SP1					
		2	Output terminated at output MPP jack SP2					
350	15E	1	Output terminated at output MPP jack SP3					
		2	Output terminated at output MPP jack SP4					
496	1F0	*	Flash Pos 1		Flash Pos 1		Flash Pos 1	
498	1F2	*	Flash Pos 1		Flash Pos 2		Flash Pos 2	
500	1F4	*	Flash Pos 1		Flash Pos 3		Flash Pos 3	

*Only one receiver is associated with special purpose bsu/biu address 496, 498, and 500

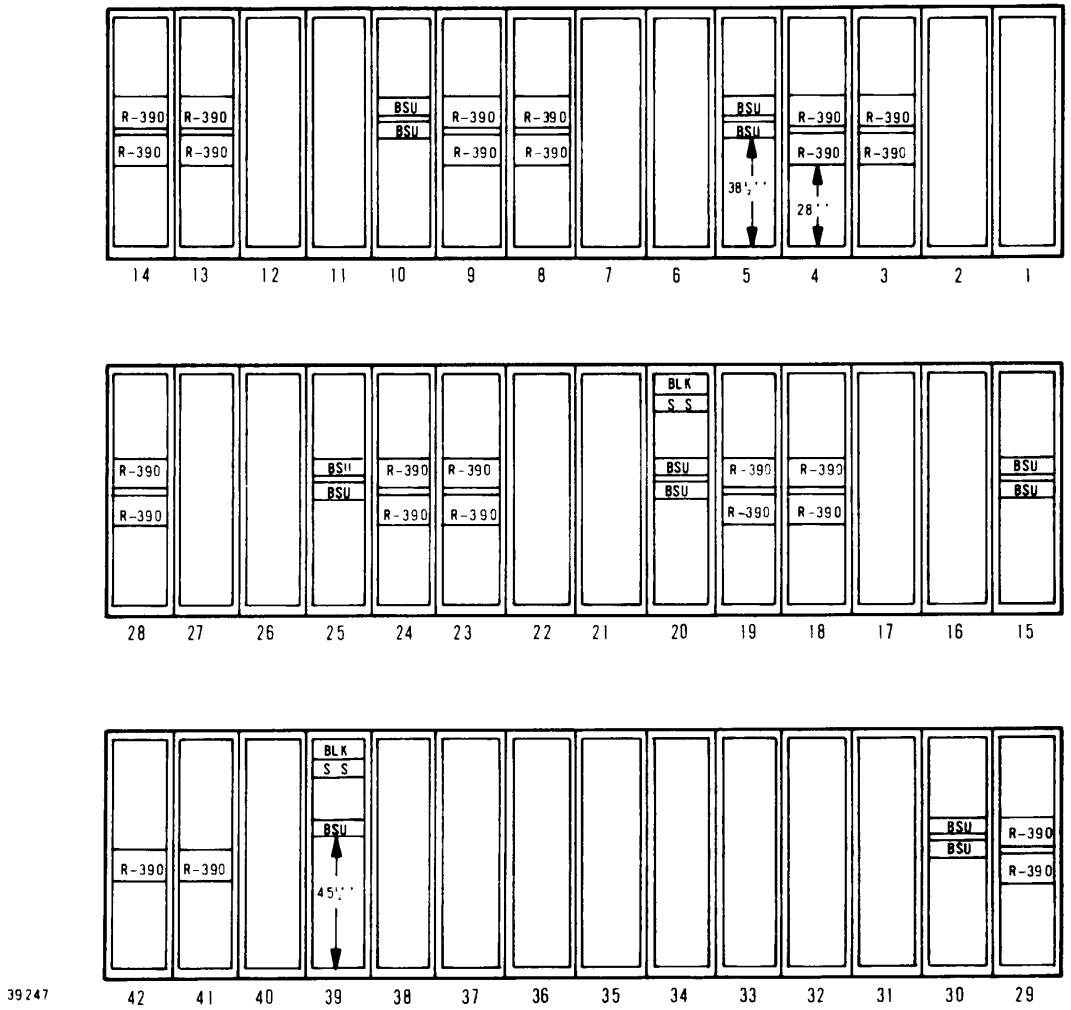


Figure 1-2. Typical Equipment Location.

1-10. List of Publications. (See table 1-7.)

List of publications required to support the intercept group equipment is listed in table 1-7.

Table 1-7. List of Publications

Title	Manual No.
Radio Receiver R-390A/URR	TM 11-5820-358-35
Electronic Voltmeter 410C	Hewlett-Packard 01556-3
Set Manual Countermeasures Receiving Set AN/FLR-9(V7)	IM 32-5895-231-15
Set Manual Countermeasures Receiving Set AN/FLR-9(V8)	IM 32-5895-231-15/1
Operating and Service Manual for Oscilloscope 140A	01638-6
Test Set, Beam Selection-Identification TS-3282/FLR-9(V)	IM 32-6625-260-14
Calibrator Beam Selection-Identificatior Unit TS-3289/FLR-9(V)	IM 32-6625-261-14

SECTION II

INSTALLATION

2-1. Scope.

This section contains unpacking, inspection, location, and installation instructions for equipment comprising the intercept group.

2-2. Unpacking.

Upon receipt of a unit, carefully open the shipping container. Check that the container is upright. Do not drive any sharp tools into seams. Inspect container for signs of damage before dismantling. After opening container, carefully remove contents. Before discarding shipping containers, determine if they should be conserved for further use.

2-3. Inspection. (See table 2-1.)

After the shipping containers have been unpacked, visually inspect the cabinet and all assemblies for defects listed in table 2-1. Repair or replace all defective items before placing unit in operation.

Table 2-1. Inspection

Item	Procedure
Chassis	Check for dented or bent frame.
Circuit Cards	Check for loose circuit cards in mating jacks. Check circuit card holder for bent runners and loose circuit cards.
Connectors	Check for bent, broken, or missing pins; distorted barrels and damaged threads; broken inserts; and damaged potting compound.
Controls	Check for damaged, loose, or missing knobs and for bent shafts.
Cables	Check for frayed or otherwise damaged cables.

2-4. Equipment Floor Space.

Intercept Group equipment (both types of bsu/biu, position scanner, and substation) are mounted in equipment racks. Refer to paragraph 1-9 for rack location and reference designators.

2-5. Installation. (See figure 2-1)

a. Bsu/Biu. Perform the following procedural steps to install either type of bsu/biu in applicable cabinets.

NOTE

A typical row of equipment is shown in figure 1-2. Equipment location is defined in tables 1-5 and 1-6 for the (V7) and (V8) sites, respectively.

1. Carefully place the bsu/biu in the cabinet from the front side of the cabinet.
2. Attach the bsu/biu to the cabinet by tightening the four attaching screws on the front panel of the bsu/biu.
3. Connect the substation signal cable to J1. See table 9-1 (Volume 2) for cable distribution.
4. Connect the power cord to a 115-volt ac outlet.
5. Connect the grounding bus to the rack grounding strap.

b. Substation. Perform the following procedural steps to install the substation in the applicable cabinet.

1. Carefully place the substation in the cabinet from the frone side of the cabinet.
2. Attach the substation to the cabinet by tightening the four attaching screws on the front panel of the substation.

3. Connect the bsu/biu signal cables to appropriate jacks (J2 through J9). See table 9-1 for cable distribution.

4. Connect the position scanner signal cable to J1.
5. Connect the power cord to a 115-volt ac outlet.
6. Connect the grounding bus to the rack grounding strap.

c. Position Scanner. The position scanner is rack mounted in cabinet 209. Refer to the system control group manual for installation.

d. Intercept Group Test Equipment.(See figure 2-la.) The Intercept Group test equipment consists of floating spare items that are installed the SOM Console for testing purposes. Installation procedures are the same as in the preceding paragraphs and initial adjustments are the same as in paragraph 2-6.

2-6. Initial Adjustments.

a. Bsu/Biu. Initial adjustments for either type of bsu/biu are contained in the following procedural steps.

1. Remove top cover from the equipment.
2. Connect the ac power cord from the bsu/biu to a 115-volt ac outlet.
3. Set the POWER switch to ON.

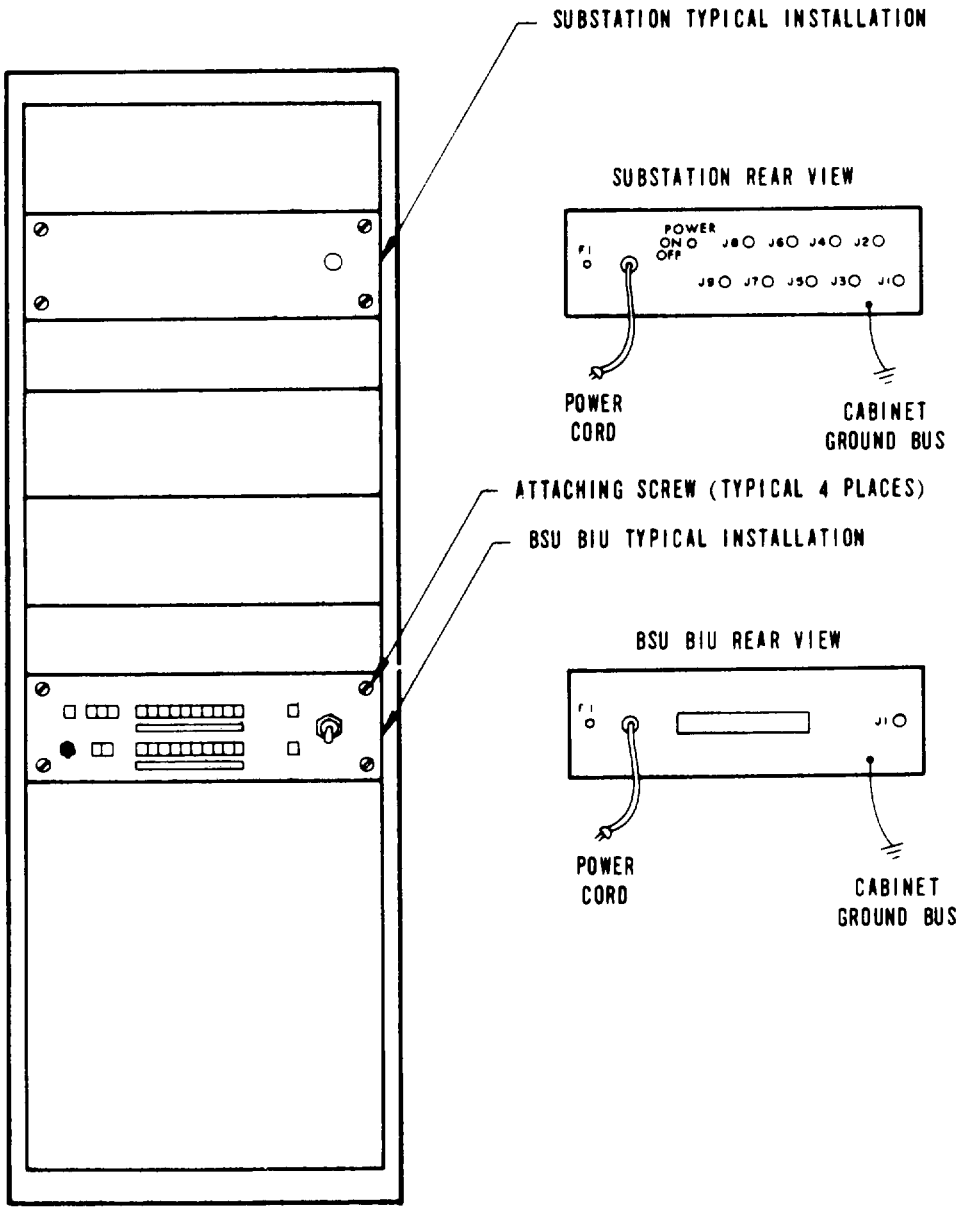


Figure 2-1. Intercept Group Equipment Typical Installation

4. Use a HP Model 410C Electronic Voltmeter to measure 5 + 0.2 volts dc between + and - terminals of the power supply (figure 5-8).

5. Adjust the power supply VOLT control (R14) for a 5 + 0.2 volts dc meter reading.

NOTE 1

The overload (O.L.) and overvoltage protection device (O.V.P.) are factory adjusted. No further adjustments should be necessary.

NOTE 2

The ADDRESS SELECT switches are hidden by a protective cover (see figure 3-1) which must be removed so that the switches may be positioned properly while placing the bsu/biu in operation. This cover must be replaced after the address is assigned to prevent unauthorized changing of the bsu/biu address.

b. Substation. The initial adjustments for the substation are identical to the bsu/biu. Repeat the steps in subparagraph 2-6.a. to adjust the substation power supply.

c. Position Scanner. Adjustments are not necessary.

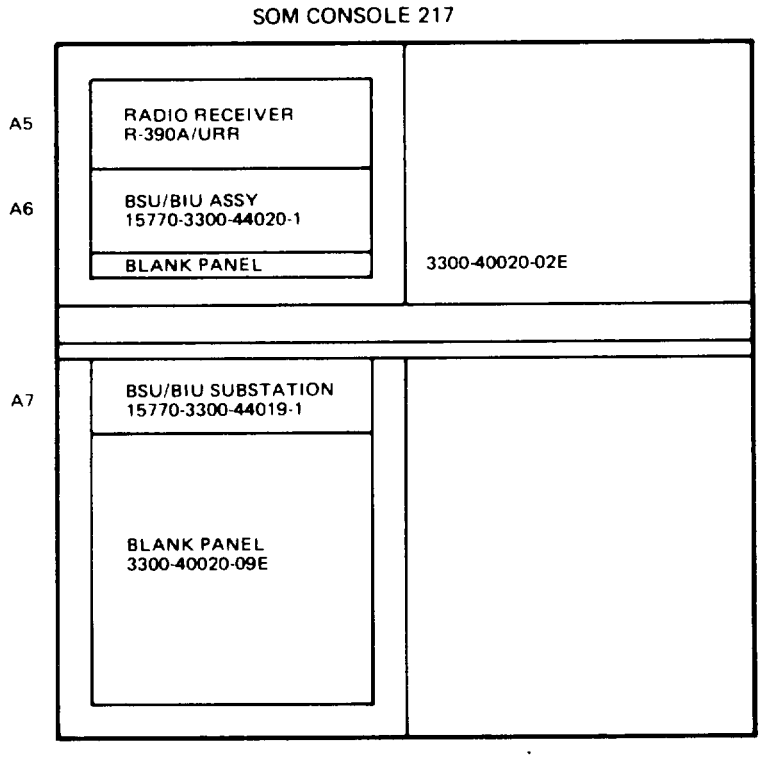


Figure 2-1a. Intercept Group Equipment Test Installation

SECTION III

OPERATION

3-1. Scope.

This section provides operating instructions for the beam select unit and beam identification unit (bsu/biu), special project bsu/biu, and the substation. Since the position scanner has no controls or indicators, no operating instructions are included.

3-2. Controls and Indicators.

a. Bsu/Biu Controls and Indicators. (See figure 3-1 and table 3-1.)

b. Special Project Bsu/Biu Controls and Indicators. (See figure 3-2 and table 3-2.)

c. Substation Controls and Indicators. (See figure 3-3 and table 3-3.)

3-3. Turn-On Procedures. (See figures 3-1 through 3-3.)

Perform the following steps to apply power to the bsu/biu, special project bsu/biu, and substation.

a. Set BSU/BIU POWER switch (S25) to ON.
b. Set special project bsu/biu POWER switch (S5) to ON.
c. Set substation POWER switch (S1) to ON.

3-4. Operating Procedures. (See figure 3-1.)

a. Perform the following steps to place the bsu/biu in operation.

1. Press and hold DISPLAY Switch (S35) in LAMP TEST. While holding the switch, observe that a figure 8 is displayed in BAND and AZIMUTH indicators.
2. Use ADDRESS SELECT switches (bits I through 9) to preset assigned hexi-decimal address in bsu/biu. Up position is binary 1, down is binary 9; switch S26 (left most switch position) is most significant bit. (See table 1-5 or 1-6 as applicable.) Remove switch cover for access to switches.
3. Momentarily press RCVR 1 (S21).
4. Observe Program Azimuth Sheet and determine BEAM SELECT code required to obtain desired azimuth and rf band.
5. Momentarily press desired BEAM SELECT switch.
6. Observe BAND and AZIMUTH indicators for verification of desired band and azimuth.
7. Repeat steps 3, 4, and 5 to provide an rf path to receiver 2.
8. If a fault or malfunction in the bsu/biu occurs, momentarily press the FAULT switch. Observe that the FAULT lamp is illuminated.

NOTE

A message is printed on the somc tty machine identifying the faulty bsu/biu when the FAULT switch is pressed. The operator number in the fault message is the bsu/biu address in decimal format.

9. If the beam connection is no longer required from the computer, momentarily press NO BEAM switch (S24) twice. Before pressing the switch the second time, be sure the rf signal is no longer present at the receiver. (See paragraph 3-7.c.) Observe that the NO BEAM lamp lights.

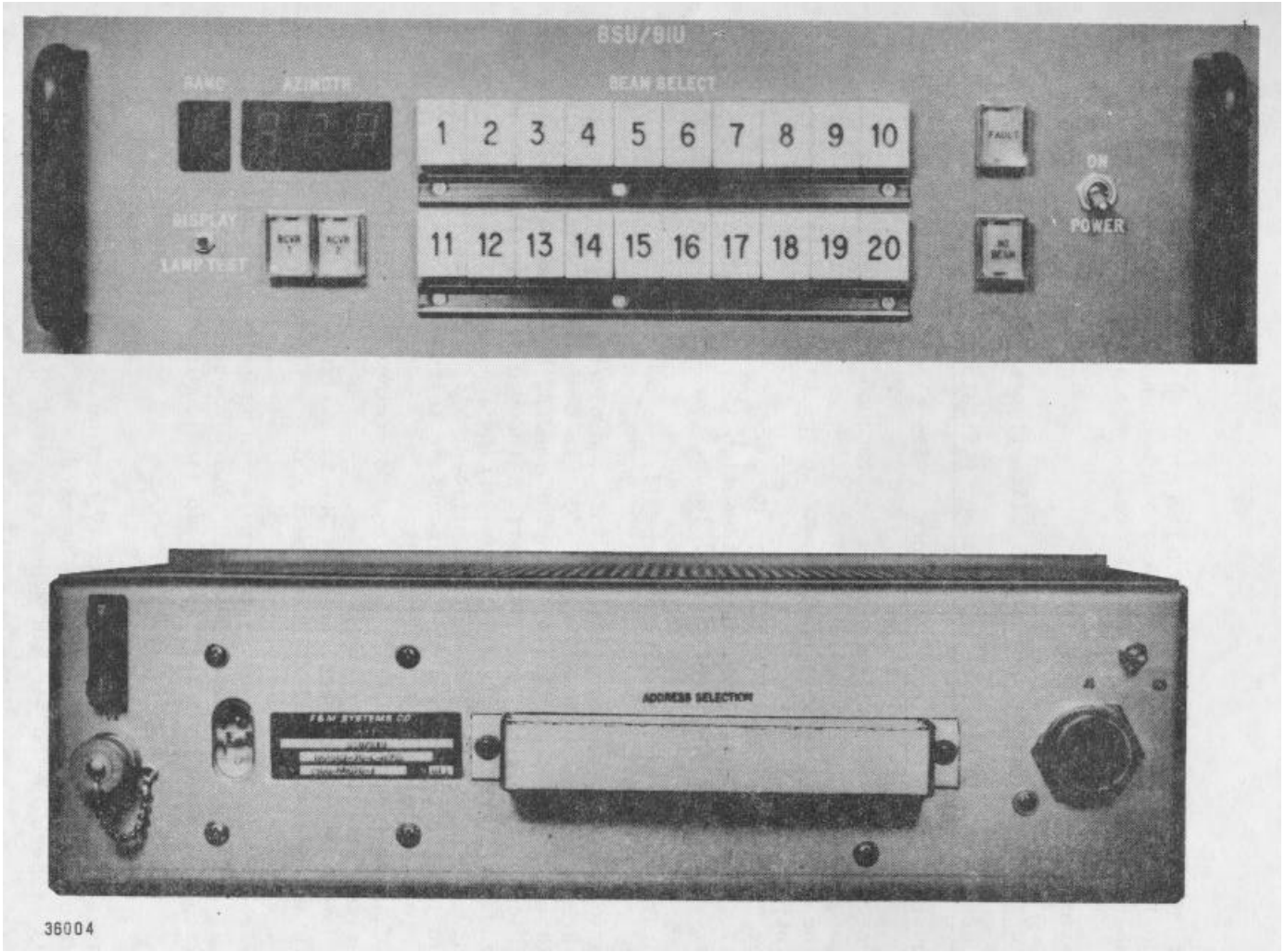


Figure 3-1. Bsu/Biu, Controls and Indicators

Table 3-1. Bsu/Biu Controls and Indicators

Control or Indicator	Reference Designator	Function
BEAM SELECT	S1 through S20	Provides a coded word to the computer signifying the computer program reference for the desired rf band and azimuth.
RCVR 1	S21	Selects receiver 1 as the recipient of the rf signal path selected by the BEAM SELECT switches. Also controls display of the azimuth and band of rf signal supplied to receiver 1.
RCVR 2	S22	Selects receiver 2 as the recipient of the rf signal path selected by the BEAM SELECT switches. Also controls display of the azimuth and band of rf signal supplied to receiver 2.
FAULT -	S23	Provides a coded word to the computer signifying to computer program reference for a fault printout at somc tty machine. Lights lamp when operator presses switch and remains lighted until the BEAM SELECT switch is pressed. . Lights lamp also when the computer fails to locate an rf path through the switch matrix and returns a high level FAULT signal to the bsu/biu.
NO BEAM	S24	Provides a coded word to the computer to break the rf connection made to the displayed receiver. Pressing once connects the input of the receiver to a 75 ohm load. Pressing the second time releases the connection for use with other beam requests. NO BEAM lamp lights when switch is pressed; lamp remains lit until a BEAM SELECT switch is pressed.
POWER	S25	Applies 115-volt ac to power supply when set to ON.
DISPLAY LAMP TEST	S35	Applies power to BAND and AZIMUTH lamps to display a figure 8 when set to LAMP TEST.

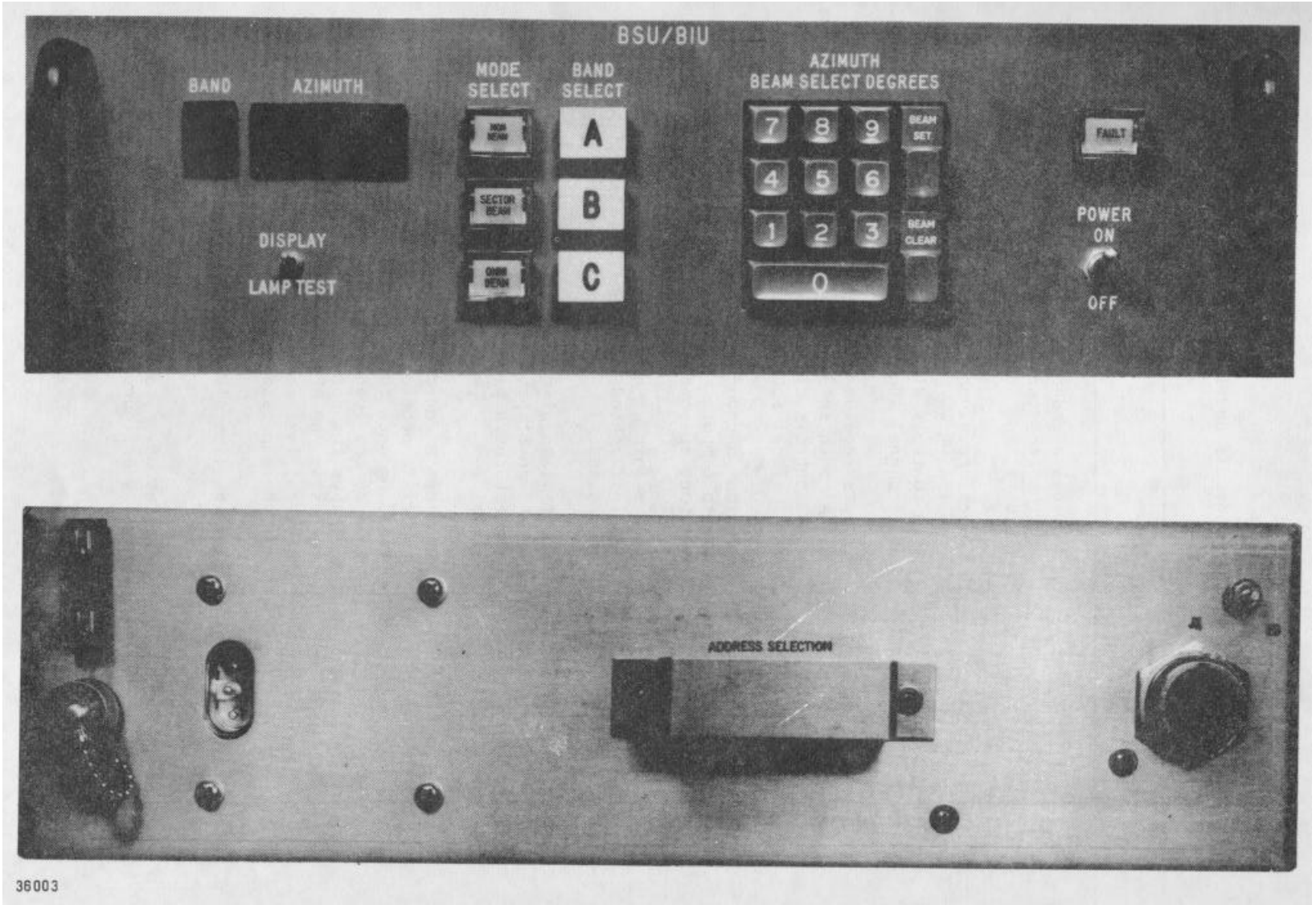


Figure 3-2. Special Project Bsu/Biu, Controls and Indicators

Table 3-1. Bsu/Biu Controls and Indicators (Continued)

Control, or Indicator,	Reference Designator	Function
BAND	DS1	Indicates rf band (Band A, B, or C in use by receiver 1 or 2).
AZIMUTH	DS2 through DS4	Indicates azimuth of rf beam in use by receiver 1 or 2.
ADDRESS SELECT 1 through 9 (Rear Panel under switch cover)	S26 through S34	Provides a 9-bit hexadecimal address word for comparison to computer generated address word. Decimal address 0 through 173 used at V7; decimal address 0 through 91, 101 through 321, 349 or 350 used at V8.

Table 3-2. Special Project Bsu/Biu Controls and Indicators

Control, or Indicator,	Reference Designator	Function
AZIMUTH BEAM SELECT DEGREES	A21	
BEAM SET	A21 S16	Initiates computer response to previously pressed switches on the same panel.
BEAM CLEAR	A21 S8	Clears stored beam request data from the local register prior to each new beam request.
0 through 9	A21, S1, 2, 3, 5, 6, 7, 9, 10, 11, and 14	Selects antenna azimuth angle in degrees, one digit at a time. First digit entered is hundreds, followed by tens, and then units.
BAND SELECT		
A	S2	Selects band A antenna
B	S3	Selects band B antenna
C	S4	Selects band C antenna
MODE SELECT		
MONITOR BEAM	A 17	Selects monitor beam

Table 3-2. Special Projects Bsu/Biu Controls and Indicators (Continued)

Control, or Indicator,	Reference Designator	Function
SECTOR BEAM	A18	Selects Sector Beam
OMNI BEAM	A19	Selects omni beam
DISPLAY-LAMP TEST TEST.	S1	Displays 8888 in BAND-AZIMUTH lamp when set to LAMP-
POWER		S5 Applies 115 volts ac to power supply when set to ON.
BAND	DS1	Indicates frequency band (A, B, or C) in use.
AZIMUTH	DS2	Indicates azimuth (hundreds digit) of signal arrival.
	DS3	Indicates azimuth (tens digit) of signal arrival.
	DS4	Indicates azimuth (units digit) of signal arrival.
FAULT	A20	Provides a coded word to the computer signifying to computer program reference for a fault printout at somc tty machine when followed by BEAM SET. Lamp lights when operator presses switch and remains lighted until the BEAM CLEAR switch is pressed. Lamp also lights when the computer fails to locate an rf path through the switch matrix and returns a high level FAULT signal to the special project bsu/biu.
ADDRESS Enter SELECTION (1 through 3)	S6 S7 S8	Used to select one of these special projects bsu/biu addresses. 000, 001, or 010 for address 496, 498, or 500 respectively.

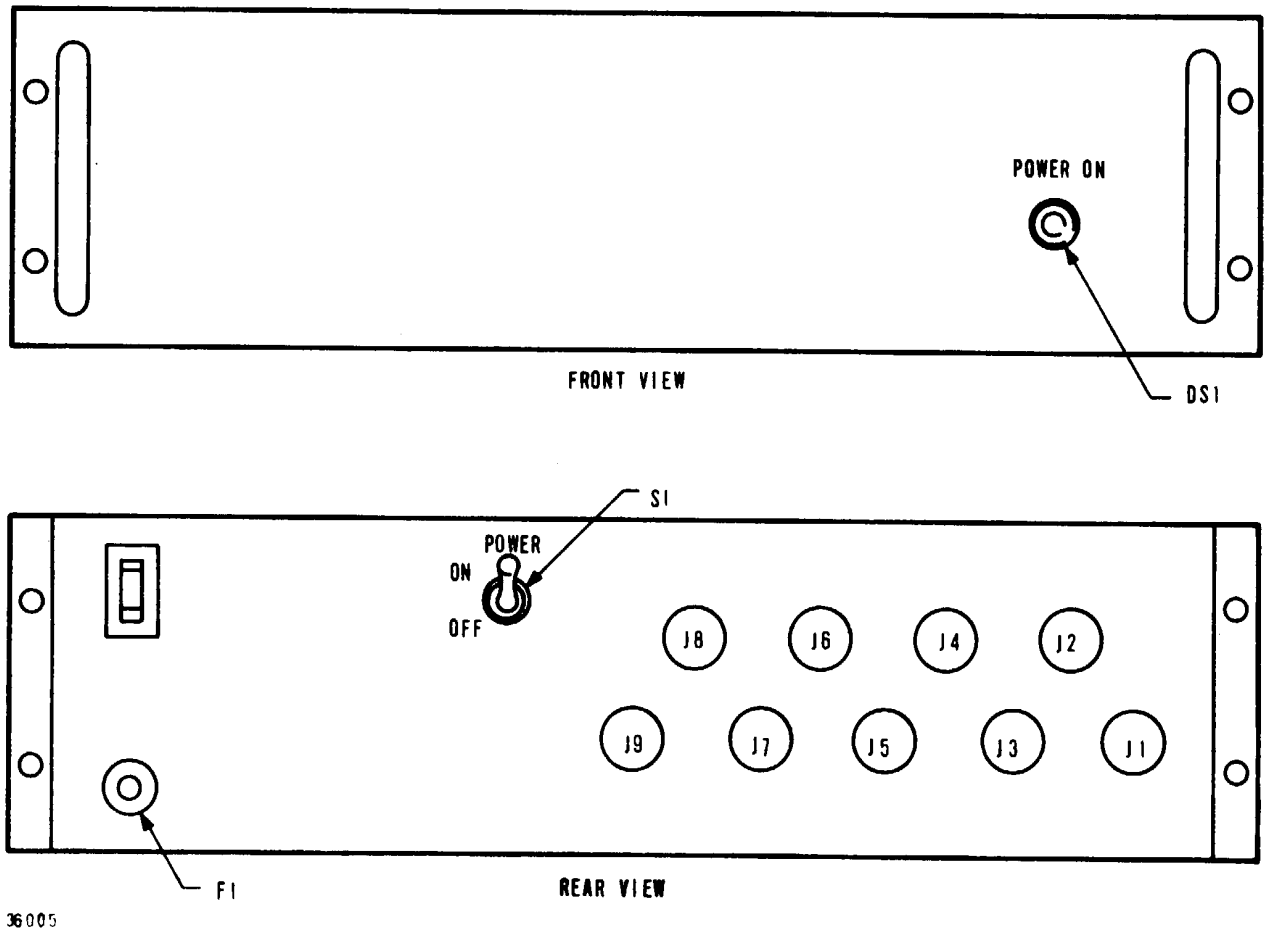


Figure 3-3. Substation Operating Controls

Table 3-3. Substation Controls and Indicators

Control, or Indicator,	Reference Designator	Function
POWER	S1	Applies 115 volts ac to power supply when set to ON.
POWER ON	DS1	Indicates 5 volts dc power is on.

b. Perform the following steps to place the special project bsu/biu in operation.

1. On front panel of special project bsu/biu, set POWER ON-OFF switch to ON.
2. Press and hold DISPLAY/LAMP TEST switch in LAMP TEST position. A figure 8 should be displayed in all sections of the BAND and AZIMUTH indicators.
3. On rear panel of special project bsu/biu (behind switch guard), set ADDRESS SELECTION toggle switches (1, 2, or 3) to preset appropriate address (up is binary 1, down is binary 0). Note that hexidecimal address 496 is internally wired and each bsu/biu uses two adjacent addresses. Therefore, the ADDRESS SELECTION switches are set to binary 000 (address 496), 001 (address 498) and/or 010 (address 500) for the three special project bsu/biu's; at the V8 site, 011 (address 502) and 00 (address 504) are available for special project bsu/biu's not installed.
4. Press and release BEAM CLEAR switch.
5. Press MODE SELECT MON BEAM, SECTOR BEAM, or OMNI BEAM switch for type of beam desired.
6. Press BAND SELECT A, B, or C switch for required band.
7. If a monitor beam is selected, press AZIMUTH BEAM SELECT DEGREES as required for desired azimuth (select hundreds digit first, followed by tens and units digits). If sector beam is selected, press 00 BEAM SELECT DEGREES switches and then either 1, 2, or 3 for the sector beam desired (001, 002, or 003). If omni beam is requested no azimuth is required.
8. Press BEAM SET switch to enable response to selection.

NOTE

Steps 4. through 8. must be performed each time BAND, AZIMUTH, or MODE SELECT switches are selected. If error is made, press BEAM CLEAR and repeat steps 5. through 8.

9. Observe BAND and AZIMUTH displays to verify correct response.

NOTE

Antenna resolution is limited by the number of antenna elements. Actual azimuth in degrees (azimuth displayed) may differ slightly from that requested. Omni beam provides a 360-degree display.

10. If response to a request is not correct, press BEAM CLEAR, FAULT, and BEAM SET switches. A message is printed out on the somc teletype, identifying the faulty special project bsu/biu which uses address 496, 498, or 500.

NOTE

A message is printed on the somc tty machine identifying the faulty bsu/biu when the FAULT and BEAM SET switches are pressed.

3-5. Turn-Off.

Set POWER switch on affected unit to OFF.

3-6. Emergency Turn-Off.

Set POWER switch on affected unit to OFF.

3-7. Bsu/Biu Operating Characteristics.

a. Introduction. Each bsu/biu has 20 BEAM SELECT switches for beam selection, 2 lighted switches (RCVR 1 and RCVR 2) for receiver selection, a lighted FAULT switch, and a lighted NO BEAM switch. In addition, there is a BAND and AZIMUTH display which provides a one-letter, three-number indication of the band and azimuth of the beam connected. The beam assignment table stored in the operating program determines which beam is selected when a given numbered switch is pressed. Each operator must have a Program Azimuth Sheet defining the beams assigned to a bsu/biu to correctly interpret the actions of beam selection at the FLR-9(V7) site. The set of 20 beams assigned to receiver I may be different from the set assigned to receiver 2; hence, up to 40 beams are available to each bsu/biu. At the FLR-9(V8) site, the set of 20 beams assigned to a bsu/biu are used for both receivers. Narrow monitor beams, 60-degree sector beams, and 360-degree omni beams may all be assigned by the beam assignment table. Omni beams display the band and an azimuth of 360 degrees. Sector and monitor beams with the same center azimuth and the same band have identical displays. Although nominal frequencies for the three bands are: A, 1.5 MHz to 6 MHz; B, 6 MHz to 18 MHz; and C, 18 MHz to 30 MHz, these are not strict rules, only guidelines, and strong signals may be adequately received at frequencies outside the frequency intervals for a given band. The beam assignment table for a given bsu/biu may include beams of all three types from one or all of the three bands. These tables can be changed by mission control to reflect changes in mission by reprogramming the data tables in the control program or on a-one-time basis through the somc tty.

b. Beam Selection.

1. Operator Beam Selection. Suppose, as an example, that an operator wants to put the band A omnibeam on receiver I and a band B 24-degree monitor beam on receiver 2. Perform the following steps. Press the switch for receiver 1; it lights. Press the switch for the band A omnibeam as shown on the Program Azimuth Sheet. The azimuth display should register A 360. The beam is then connected to receiver 2. Press the switch for receiver 2; it lights. Receiver 1 is still connected but is not displayed. Press the switch that corresponds to the band B 24-degree monitor beam on the Program Azimuth Sheet for receiver 2. The display should read B 024. Both receivers are now connected. To change a beam, simply make certain that the switch is lighted for the receiver whose beam is to be changed. Select a different numbered button corresponding to the new beam. The other receiver is unaffected. Changing receiver switches without pushing numbered switches has no effect other than displaying the beam currently connected to the receiver selected.

2. Computer Controlled Adjacent Beam Selection. Because of blocking introduced in the switch matrix as a result of previous path verification failures, it may not be possible for the computer to find a path which will connect a requested beam to an operator. In the event that the computer is unable to connect a requested monitor beam to an operator because of blocking encountered in the switch matrix, it will automatically attempt to connect the operator to one of the two monitor beams adjacent to the originally requested beam. The first attempt is made to connect the operator to the adjacent beam in the counterclockwise direction. If blocking is also encountered here, an attempt is made to connect to the adjacent beam in the clockwise direction. Path verification is done on the adjacent beam just as would have been done on the original beam. If an adjacent beam Is successfully connected to the operator, the azimuth of the adjacent beam is displayed to the operator. Thus, as a result of the "ping-pong" beam selection action, the operator may receive an azimuth display of a monitor beam adjacent to the one he requested. This is an indication the computer has encountered blocking and has selected an adjacent beam for the operator. No other indication is given. If blocking is encountered on both adjacent beams, as well as the originally requested beam, no connection is made and a fault light and blank display are output to the bsu/biu and the message SWITCH BLOCK AT PORT $XXX is output to the tty. If blocking is encountered on an omni or sector beam request, no adjacent beam Is possible, so a fault light and blank display are output to the bsu/ biu and the message SWITCH BLOCK AT PORT $XXX Is output to the tty.

c. NO BEAM Switch. The switch marked NO BEAM lights when pressed. Pressing the button once terminates the receiver selected with a 75-ohm resistance (switch matrix input pin 160). This feature is useful for receiver maintenance and alignment. Pushing the switch a second time removes the path record from the computer table. The connection Is freed to be used by other beam requests from other bsu/biu's. When a position is not going to be used for an extended period, the NO BEAM switch should be pressed twice to free the switch matrix crosspoints for other users. To be effective the first depression of the switch must be answered before the switch is pressed again. Therefore, the operator should wait until the 75-ohm termination is made (loss of received signal) before pressing the NO BEAM switch the second time.

d. FAULT Switch. The FAULT switch lights to indicate one of the following: (1) path verification failure, (2) antenna beam to receiver path broken, (3) at FLR-9(V7) site only, switch matrix card removal imminent, (4) unassigned beam select switch, (5) invalid bsu/biu address, (6) bsu/biu failure, and (7) operator presses the FAULT switch. Illumination of the FAULT light Indicates that something may have happened or something Is going to happen which affects the rf signal connected to one of the user receivers, without designating which one. However, all such occurrences affecting the rf signal may not be accompanied by the FAULT light. The following paragraphs describe conditions leading to a lighted FAULT switch and the actions to be taken by the operator.

1. Path Verification Failure. When an operator selects a beam by pressing a beam select switch, three crosspoints must be closed in the switch matrix by the computer. The path verification routine then checks that the rf signal is successfully connected. If one of the crosspoints is faulty, a valid path verification can not occur. Instead of getting the beam requested and its display, the FAULT switch lights and the display is blank. The operator should again request the beam by pushing the appropriate switch. Normally, the fault light and blank display are replaced by the requested beam-azimuth display. In the event that an operator receives repeated faults in trying to select a beam, an adjacent monitor beam, a sector beam, or

an omni beam should be tried which serve to monitor the mission. If this proves impossible, there is probably a failure in the receiver's switch matrix output card. The FAULT switch should be pressed. The somc operator should note path verification failure followed by operator fault and take appropriate action by testing the A3 matrix of the receiver using TEST RFSM PATH XXX, YYY and having a failed card removed for testing and replacement. The operator should change to the other receiver and resume mission on that receiver. The somc operator should notify the operator when the card for the disabled receiver has been replaced. Since each FAULT light indication is accompanied by a printed message, no more than four occurrences should be caused: two for the beam desired, one for an alternate beam, and one by actually pushing the FAULT switch to notify the somc operator that maintenance assistance is required. There may be occasions when path verification failure is caused by an olm εt failure. In this event, both a beam and a fault light is displayed. (A message PATH VER VOID is printed at the somc.) Under these circumstances, it is expedient to assume that the displayed beam is usable, since it, in fact, is connected.

2. Antenna Beam to Receiver Path Broken. If a path through the switch matrix is broken, the operator, upon noticing this, should press the FAULT switch. (Beam loss could be caused by component failure or switch matrix card removal.) It may not be possible to tell when a path has been broken except by monitoring the receiver. if a given receiver has a broken path, when the somc operator pushes the RFSM OLM&T test, the FAULT switch lights notifying the operator that his beam has been lost. If the FAULT light comes on without the operator initiating any action at the bsu/biu, the beam should be requested again since the FAULT light Indicates either that the beam has been lost, or at the FLR-9(V7) site only, that it soon may be lost.

3. Card Removal Imminent. Before the somc operator removes a card from the switch matrix, a command is input (STAGE X SUBMATRIX YY OUTPUT ZZ REMOVED) to avoid connecting new paths through that card. Simultaneously, at the V7 site, all operators whose beams will be lost when the card is physically removed get a lighted FAULT switch to warn that beam loss is imminent. At the V8 site, the card removal is indicated only by the loss of rf signal with no FAULT light output. At both sites each operator should reselect the beam to obtain a path around the card removed from service by the STAGE REMOVED command. In the event that the removed card is the output card for that receiver, the stage removed command is not necessary; no beam selection is possible until the card has been replaced and the somc operator should advise the mission operator of the circumstances.

4. Unassigned Beam Select Switch. It is possible to have beams listed in the beam assignment table for a subset of the 20 numbered switches. Any unassigned switch yields a FAULT light and a blank display when pressed.

5. Invalid Bsu/Biu Address. The hexadecimal address of the bsu/biu is set using a set of toggle switches. Not all possible addresses are valid. An invalid address causes all beam requests from that bsu/biu to be answered by a FAULT light and a blank display. Each operator, therefore, in addition to his bsu/biu beam assignment table, should know the unique configuration of toggle switches which constitute the valid address of that bsu/biu.

6. Bsu/Biu Failure. It Is possible for the logic hardware of a bsu/biu or substation to fail, causing FAULT light indicators and/or blank display in answer to beam selections. Some types of failures can cause severe program distress, thus defective units must be removed as soon as a hardware defect is noted. Procedures for

removing and replacing bsu/biu and substation units are provided in the Intercept group manual. The somc operator should be alert for effects caused by defective bsu/biu or substation unit and direct replacement and maintenance.

7. Operator Presses FAULT Switch. When the operator presses the FAULT switch, an error message giving the position and receiver number is printed at the somc tty with the special designator @ to indicate that the switch was pressed by the operator rather than lighted by the program. The somc operator should communicate with the operator to determine the nature of the problem and take action to correct it. The operator should press the FAULT switch when he is unable to select a beam or when a path is broken while being monitored. The only effect of pressing a FAULT switch is to notify the somc operator by a printed error message that there is a problem.

e. Connecting Bleams Not in Beam Assignment Table. It is possible to connect any beam to any bsu/biu, even if it is not on that unit's beam assignment table. The somc operator may assign a beam connection individually using the instruction OPER XXX, Y BEAM ZZZ. Several bsu/biu's may be given one-time beam connection from the tty using INPUT RFD P and a paper tape. The somc operator may assign a one-time beam connection to every bsu/biu by using INPUT RFD M, X, Y, VVVVVVVV and a magnetic tape table. When multiple bsu/biu connections are made from the tty, the beams connected may be different for each receiver. In all cases, when a beam is connected to the bsu/biu by the tty operator on a one-time basis, the band and azimuth will be displayed, but the FAULT and NO BEAM switches, if lit, will remain lit. The connection nonetheless has been made if the band azimuth display shows the appropriate values. Any beam selection from the bsu/biu loses the beam connection that was initiated by the tty input command. The beam connection may only be reinstated by action at the tty.

f. Operating Tips.

1. Beam Request Servicing. The position scanner looks at each bsu/biu every 51.2 milliseconds. Normally, therefore, a single push of a switch should bring a rapid response. If a response fails to occur, press the switch after 15 seconds or so. Do not repeatedly push the switch rapidly. This may contribute to an operating program overload, and at minimum cause an error message printout.

2. Computer And/Or Switch Matrix Failure.

(a) Computer Failure. If the computer halts, no beam requests are processed. All beams connected prior to the failure remain connected so long as the switch matrix is not accessed by transients.

(b) Switch Matrix Failure. The switch matrix is designed to provide paths around faulty crosspoints. However, if faults do occur wherein an alternate path is not available, a signal is sent to the requesting bsu/biu providing a FAULT light and blank azimuth display. Output ports in the switch matrix are devoted to user positions. If a failure exists in one of these ports, there is nothing to be done until the fault is corrected. A power failure in the switch matrix may cause the switch matrix to arbitrarily break previously made paths. Therefore, after a switch matrix power failure, all beams should be reselected when power is restored.

(c) General. Due to the preceding stated faults, the somc operator should notify the mission operators of computer failure and switch matrix failure and the

subsequent repair of these devices. Mission operators having critical beam selections should determine the system status prior to requesting any changes in the rf path.

3. Path Verification Inhibited. BAND and AZIMUTH display will appear following valid beam requests when the path verification test is inhibited. It is possible for the path connections to be faulty under these circumstances. If connections appear to be faulty, reselect beam; and if still faulty, notify the somc operator.

3-8. Special Project Bsu/Biu Operating Characteristics.

a. Introduction. These units have the ability to select all monitor beams, the three sector beams, and the omni beam in each band. The operating characteristics are similar to those of the bsu/biu except in those areas discussed in the following paragraphs.

b. Panel Layout. The control panel includes the band/azimuth display; a FAULT switch; switches for selecting monitor beam, sector beam, and omnibeam; three band select switches; a 0 through 9 keyboard array; a BEAM SET switch; and a BEAM CLEAR switch. The MONITOR-SECTOR-OMNI switches light when pressed. The band azimuth display set indicates which band and what azimuth has been connected to the associated receiver. The beam type switch which is lighted indicates the monitor, sector, or omni beam which has been selected.

c. Beam Selection Procedure.

1. Operator Beam Selection. To make a beam request, the following procedures must always be followed.

(a) Press BEAM CLEAR. This turns out all the indicators, e.g., FAULT switch.
(b) Press the appropriate beam type switch for the beam desired (MONITOR, SECTOR, MONI).
(c) Press one of the band switches (A, B, or C).
(d) Press the appropriate numbered switch for the azimuth desired. For monitor beams, select a 1-, 2-, or 3-digit azimuth in sequence, i.e., 123 degrees is requested by pushing the I switch, then the 2 switch, then the 3 switch. The azimuth displayed is rounded to the nearest actual monitor beam and that is the beam connected. Requests from 360 degrees to 400 degrees yield a FAULT light. A hundreds digit of 4 is interpreted as 0; 5 as 1; 6 as 2; and 7 as 3. Beam requests outside the range of 0 to 360 degrees are not useful and are not to be used. For sector beams select either 001, 002, or 003. Any other request yields a FAULT light. For omni beams, no azimuth is required.
(e) Press the BEAM SET switch. This causes the accumulated data to be reset and initiates beam selection.
(f) If a mistake is made in steps a. through e., simply press BEAM CLEAR and repeat steps a. through e.

2. Computer Controlled Adjacent Beam Selection. Because of blocking introduced in the switch matrix as a result of previous path verification failures, it may not be possible for the computer to find a path which will connect a requested beam to an operator. In the event that the computer is unable to connect a requested monitor beam to an operator because of blocking encountered in the switch matrix, it will automatically attempt to connect the operator to one of the two monitor beams adjacent to the originally requested beam. The first attempt is made to connect the operator to the adjacent beam in the counterclockwise direction. If blocking is also

encountered here, an attempt is made to connect to the adjacent beam in the clockwise direction. Path verification is done on the adjacent beam just as would have been done on the original beam. If an adjacent beam is successfully connected to the operator, the azimuth of the adjacent beam is displayed to the operator. Thus, as a result of the "ping-pong" beam selection action, the operator may receive an azimuth display of a monitor beam adjacent to the one he requested. This is an indication the computer has encountered blocking and has selected an adjacent beam for the operator. No other indication is given. If blocking is encountered on both adjacent beams as well as the originally requested beam, no connection is made and a fault light and blank display are output to the bsu/biu and the message SWITCH BLOCK AT PORT $XXX is output to the tty. If blocking is encountered on an omni or sector beam request, no adjacent beam is possible, so a fault light and blank display are output to the bsu/biu and the message SWITCH BLOCK AT PORT $XXX is output to the tty.

d. FAULT. The action of this switch is the same as for the bsu/biu except that BEAM SET must be pressed before the FAULT switch setting is sensed and acted upon. Any time the BEAM SET switch is pressed while the FAULT switch is lighted, a fault message is printed at the somc. The actions of the computer which turns the FAULT light on are the same as for the bsu/biu. Note that because it is necessary to press BEAM CLEAR to make a new beam selection as a result of a FAULT light, the FAULT light can be lost without actually generating a new beam request.

SECTION IV

THEORY OF OPERATION

4-1. Scope.

This section contains theory of operation of the intercept group from a primary signal flow concept, The description Includes the bsu/biu, the special project bsu/ biu, the substation, the position scanner, and a common 5-volt dc power supply used in each; the bsu/biu, special project bsu/biu, and the substation.

4-2. Intercept Group Functional Description. (See figure 4-1.)

a. The two receivers at each mission operator position are supplied antenna beams by the switch matrix. The antenna beam is requested by the operator at the bsu/biu by pressing 1 of the 20 BEAM SELECT switches and the special project bsu/biu by pressing the appropriate AZIMUTH SEAM SELECT DEGREES switches. The pressed switch provides a coded word to the position scanner through the associated substation.

b. The position scanner relays the coded word and the address of the bsu/biu making the request to the system control group computer. The computer stores the position address, then performs a routine to determine the azimuth of the beam and frequency band requested. From azimuth and frequency band (band A, B, or C) the computer selects appropriate crosspoints in the switch matrix.

c. The resulting crosspoint codes select the rf path through the switch matrix to provide the receiver with the desired azimuth and frequency band. The rf signal is supplied to the receiver through a 3 10.3-dB attenuator.

d. The AN/FLR-9(V7)/(V8) Monitor and Test Group (monitor and test group) automatically monitors the selected rf path amplitude. In cases where the amplitude is not within tolerance, another rf path is selected by the computer. In cases where the amplitude is satisfactory, the computer generates an rf path verification signal.
If blocking occurs in the switch matrix, a blanking signal and a fault signal are generated.

e. The verification signal, consists of a two-word sequence; a 9-bit word identifying the address of the bsu/biu which made the request and a 14-bit binary word identifying the azimuth, the band, and the receiver in use, or a fault (if one exists).

f. The computer transmits a 9-bit address word to the position scanner followed by the 14-bit azimuth/band word. The position scanner accepts the two words during the first three phases of a five-phase Internal clock, and sends them to the appropriate bsu/biu during the last two phases. (The sequential scanning of the positions by the scanner is uninterrupted as 40 microseconds of each scan is reserved for the purpose of returning verification words received during the first 60 microseconds of the scan.) g. The bsu/biu stores the information contained in 12 bits of the 14-bit azimuth/ band word in a display storage register. Alphanumeric display of the stored azimuth, band, and receiver data is provided to the operator upon request.

4-3. Intercept Group Principles of Operation. (See figure 4-2.)

The position scanner continuously addresses each bsu/biu. Any bsu/biu requiring a beam selection produces a request signal upon being addressed. This request signal

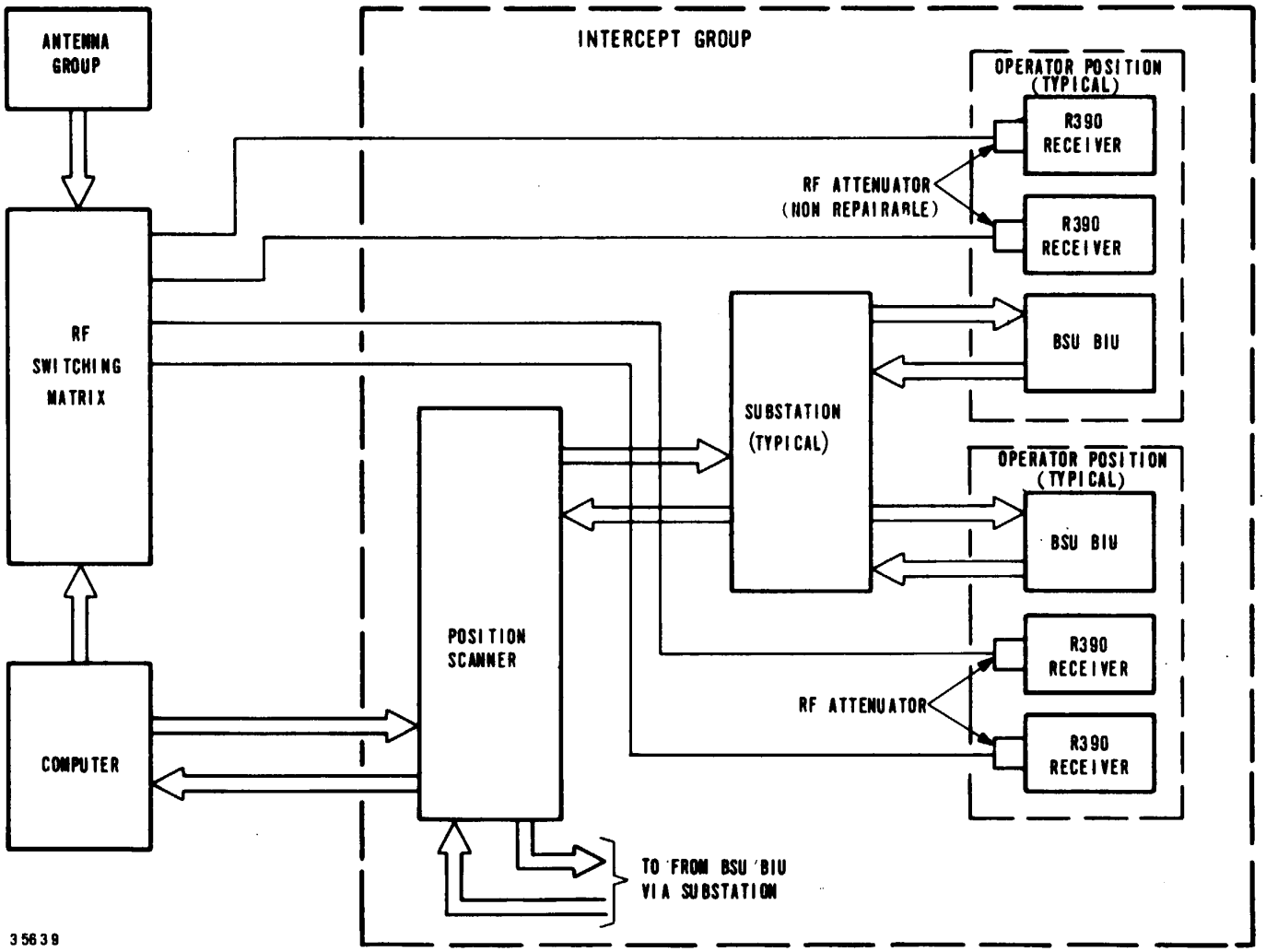


Figure 4-1. Intercept Group Block Diagram.

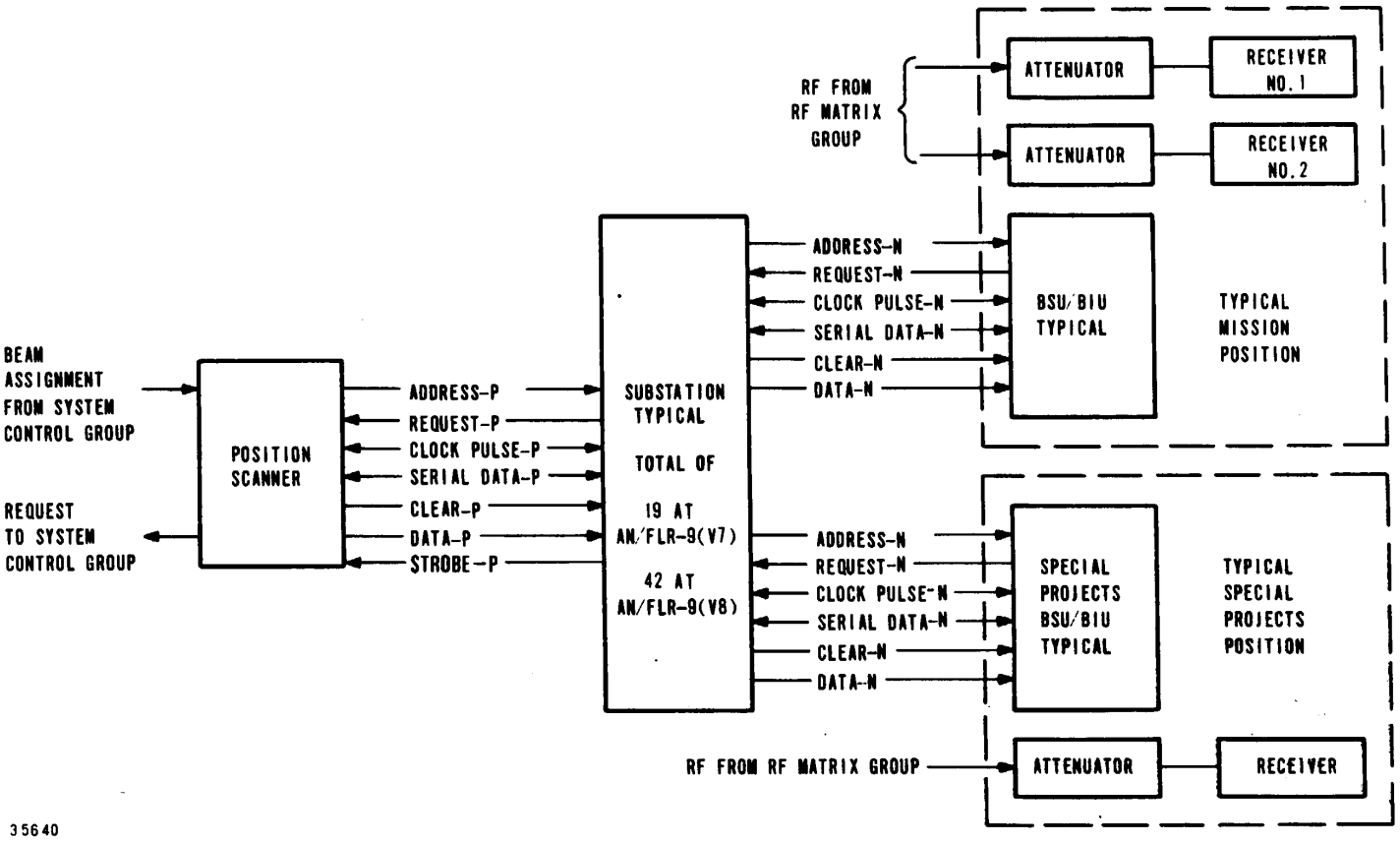


Figure 4-2. Intercept Group Simplified Block Diagram

is detected by the position scanner which then generates a series of clock pulses. The clock pulses serially shift the bsu/biu serial data into the position scanner. The message represents a band, beam, and azimuth request for the selected receiver. The position scanner routes this message to the computer. Upon receiving verification from the computer, the position scanner produces two control signals to clear the registers in the bsu/biu and to identify the following serial word as data. These messages and control words are coupled to all bsu/biu [134 in the AN/FLR-9(V7) site and 317 in the AN/FLR-9(V8) site and to special project bsu/biu 3 each in the AN/FLR-9(V7) and AN/FLR-9(V8) sites simultaneously. This type interface allows the use of an intermediate buffer to multiplex one source to numerous users. The multiplexing is accomplished in the substation [20 in AN/FLR-9(V7) site and 43 in AN/FLR-9(V8) site. This circuit receives the common data message from the position scanner. Buffer and distribution amplifiers distribute this single input to eight users (bsu/ biu). Signal lines from these eight bsu/biu are attached to the substation. The output of the addressed bsu/biu is buffered to a common output. This common output is returned to the position scanner.

4-4. Power Distribution. (See figures 7-2 and 7-3.)

Power distribution of all bsu/biu and the substation is limited to internal distribution of dc power. This power is supplied by a common type power supply to circuit boards and to displays in each unit. Power is supplied to the position scanner by two parallel power supplies located in cabinet 209.

4-5. Bsu/Biu Detailed Description.

a. Principles of Operation. (See figure 4-3.)

1. Interrogation. The position scanner continuously interrogates all bsu/biu by sequentially shifting a 9-bit serial binary address word (SERIN) to the address recognition circuits of each bsu/biu. Up to 512 discrete position addresses can be generated in the position scanner. The address word is followed by an address validate (ADDRESS) pulse which allows the addressed position to detect the address as valid. The ADDRESS pulse also allows the addressed position to return a beam service request (REQUEST) if one has been requested by the operator since the last scan of the position scanner.

2. Request. A request is produced only when the operator presses one of the 20 BEAM SELECT switches in the beam select matrix. The selected switch produces a 5-bit word and an OR signal. The design of these switches is such that the numerical values are logically ORed when two switches are simultaneously pressed. The OR signal triggers a one-shot to produce a 5-millisecond LOAD-P signal. LOAD-P signal loads the 5-bit beam select word in the beam select storage register. LOAD-P also gates a flip-flop to produce a RQST-P (request) signal. When interrogated, the position scanner serially shifts a 9-bit address word SERIN (serial-in) into the shift register. This address word is compared to the preset address of the bsu/biu in the address matrix. When these two are identical, the address matrix is enabled to produce ADORCMPR-N (address compare). This signal is produced upon receipt of the ADDRESS-N signal generated by the position scanner. The ADDRCMPR-N signal is produced following the 9-bit address word comparison to identify a successful address search. The ADDRCMPR-N signal and the previously generated RQST-P signal are applied to the request control circuit. Upon receipt of these two signals, a low level REQUEST-N signal is produced and coupled through the substation to the position scanner. ADDRCMPR-N and ADDRESS-N arriving simultaneously at the clear control circuit

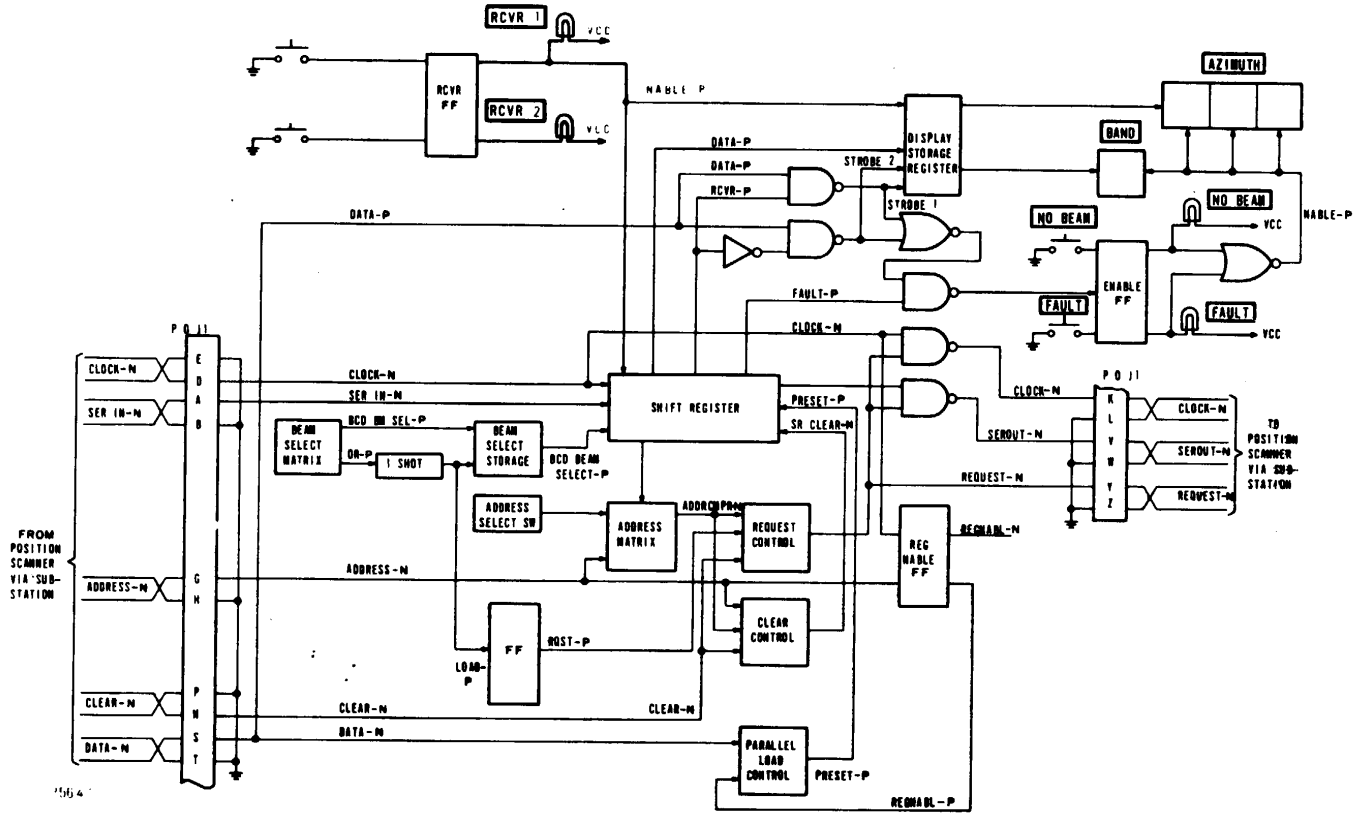


Figure 4-3. Bsu/Biu Block Diagram

produce SR CLEAR-N (shift register clear). SR CLEAR-N clears the shift register preparatory to parallel loading data stored in the beam select storage register.

3. Beam/Band Request. REQUEST-N is coupled to the position scanner through the bsu/biu substation. At this time, a DATA-N pulse is produced and coupled to the bsu/biu. The DATA-N pulse in conjunction with REGNABLE-P and REQUEST-N signals produce the PRESET-N pulse. PRESET-N parallel loads the 5-bit beam select word and a single-bit receiver-in-use word into the shift register. After being loaded, the shift register data is serially shifted out of the register and to the position scanner by seven clock pulses produced by the position scanner to load its register with the serial data word. Upon receipt of the serial data, the position scanner sends a CLEAR-N pulse to the bsu/biu, produces an interrupt signal for the computer and loads the position address into a parallel register along with the received data. Upon recognizing the interrupt signal, an External Data Input (EDI) signal is produced by the computer. The EDI signal is coupled to the position scanner. Upon receipt of the EDI signal, the position scanner couples the word containing the position address and the beam request information to the computer. In the bsu/biu, the CLEAR-N pulse produces SR CLEAR-N to clear the bsu/biu shift register. After coupling the beam request data to the computer, the position scanner continues interrogating the remaining bsu/biu's.

4. Switch Path Selection. Upon receipt of the 7-bit beam request signal, the computer performs a program routine to determine which rf path through the switch matrix satisfies the receiver, rf band, and azimuth request. The rf path is checked by the monitor and test group which is monitored by the computer while rf signals are coupled directly to the receiver associated with the requesting bsu/biu. After the computer verifies the rf path, a routine is performed to produce a 14-bit data word identifying the azimuth, band, receiver in use, or a fault, if one exists. The 14-bit word is coupled in parallel bit format to the position scanner, and from it (serially) to the requesting bsu/biu.

5. Reply. After the position scanner receives the data word and bsu/biu address from the computer, it again addresses the requesting bsu/biu, then sends the reply message. The reply message is a 14-bit data word identifying either the beam, band, and receiver in use, or a fault, if one exists. The 14-bit word is serially shifted into the bsu/biu shift register by 14 clock pulses (CLOCK-N). The 14-bit binary word stored in the shift register contains three BCD signals to light the appropriate elements in the three AZIMUTH indicators; a 2-bit word to light the appropriate BAND indicator; a single-bit word to identify the receiver in use; and a single-bit word to identify a FAULT. The FAULT signal is generated by the computer when an rf path cannot be established. This signal lights the FAULT lamp. The 10-bit AZIMUTH word and 2-bit BAND word are stored in the display storage registers. One storage register stores the BAND and AZIMUTH signals for receiver number 1 (RCVR 1) while the other storage register contains the same type signals for receiver number 2 (RCVR 2). The single-bit RCVR signal enables the loading of one of these storage registers. When RCVR is low, receiver number 2 shift register is loaded. Therefore, upon receipt of the fourteenth serial data bit, RCVR-P enables the loading of one of the shift registers. At this time the azimuth and band of the rf signal coupled to the receiver in use is stored in the shift register.

6. Beam/Band Display. The azimuth and the frequency band of the rf signal assigned to each receiver is displayed in the AZIMUTH and BAND indicators. The operator selects the display by pressing RCVR I or RCVR 2 switches. The pressed

switch lights the associated lamp and sets the receiver toggle. The resultant output of this toggle enables the appropriate display storage register to parallel load the AZIMUTH and BAND indicators. The anable flip-flop produces a level, enabling the indicators to light. The lighted indicators thereby provide azimuth and frequency band of the assigned rf signal.

7. Fault/No Beam.

(a) When an azimuth-band request cannot be supplied, the computer causes a fault message to be typed on the tty machine using the following format.

PATH VER FAILURE OPER XXX, RCVR Y BEAM ZWW

Where:
X = the operator number (decimal)
Y - the receiver number
Z = the band
W = beam number.

It also causes a coded word to be serially shifted to the requesting bsu/biu which causes the FAULT lamp to light and the BAND AZIMUTH display to be extinguished. The FAULT switch also may be pressed by the operator when he suspects an existing fault. In this case a coded message is serially shifted to the computer and the message described previously is printed on the tty machine.

(b) The NO BEAM switch is pressed once by the operator when a 75 ohm termination is desired, and twice when the receiver is not going to be used for a period of time. This action causes a coded message to be serially shifted to the computer. Upon receipt of the first message, a path through the switch matrix to input pin 160, a 75 ohm termination, is established. Receipt of the second such message causes the record of the connections to the 75 ohm termination to be erased from memory, freeing switch matrix crosspoints for use by active receivers. When the receiver is going to be idle for an extended period, and the NO BEAM switch pressed twice, the first press should be acknowledged by the loss of the rf signal due to the successful connection to input pin 160, before the NO BEAM switch is pressed the second time.

b. Electronic Circuits. (See figure 7-4,)

1. Address Recognition. The position scanner queries the bsu/biu by clocking in a 9-bit binary address code on the SERIN signal line. The address code is stored in the shift register and then compared to a preset address code. The preset address is selected by setting ADDRESS SELECT switches (S26 through S34)The three address select switches (56, S7, and S8)provide three selected bits (1, 2, and 3) used in the two word address scheme of the special projects bsu/biu. The five most significant bits of the nine bit address are prewired in such a manner as to require five high level bits in these positions. The next three significant bit positions are the three selected bits provided by the address select switches requiring bits 000 through 111. The least significant bit of the nine bit address is arranged so as to require a low level (0)for the first address word or a high level (1) for the second address word. This requires that the first address word be

111110000
through
111111110

By converting the binary address to decimal (summing the binary weights) the first address word in decimal is 496 through 510. The second address word indexes the numerical value by one when the least significant bit is changed to a high

level. This requires that the second address word be

111110001
through
111111111

which provides decimal address 497 through 511. Actual addresses at both V7 and V8 sites are decimal 496, 498, and 500 for the initial address and 497, 499, and 501, respectively, for the second address. The address code is compared to the preset address in the exclusive-OR matrix. In instances where the address code matches the preset address, the two inputs to each exclusive-OR gate are dissimilar. The dissimilar inputs produce a high-level output at each gate. The resultant high-level outputs are summed together in NAND gate 1G4D to produce ADB-N. Inverted ADB-N and the output of 1F4D (ADB9-P) partially enable the address compare gate (1G3C). The low-level ADDRESS-N signal is produced by the position scanner. The low-level ADDRCMPR-N signal, therefore, signifies that an address search has been conducted by the position scanner, and the address has been identified.

2. Request. After the address of the bsu/biu is recognized, a request signal is generated. The request signal generation is initiated by pressing one of the 20 BEAM SELECT switches (S1 through S20) and one of the receiver switches, RCVR 1 or RCVR 2 (S22 and S21, respectively). RCVR 1 switch or RCVR 2 switch produces a high or low NABLE 1 in the flip-flop comprised of NAND gates 2H7A and 2G7A. The state of NABLE 1 (high-level or low-level) determines the receiver in use. The signal is applied to the shift register (SR1D5A) in the ninth bit slot. Pressing any one of the BEAM SELECT switches applies a low level signal to the OR-N bus. The resultant OR-N signal generated in the beam request matrix is inverted by inverters 1B8A and 2D6A and applied to a differentiator and limiter consisting of A4R3, A4CR1, and A4C5. The differentiator blocks any chatter voltage as a result of the switch action while the limiter restricts the positive voltage swing to +5 volts. The negative output pulse of the differentiator is inverted by inverter 2D6B to trigger 5millisecond one-shot 2D5A. The resultant low-level output pulse LOAD-N loads the 5-bit BCD beam request data word into beam select register consisting of SR1B5A and SR1B4A. The high-level output pulse, LOAD-P, enables the fault NAND gate 2B4A and the no beam NAND gate 2C4A. These two gates are now enabled to produce a negative pulse upon receipt of a FAULT or NO BEAM S1GNAL. This low-level pulse clears the respective toggle. High-level output pulse LOAD-P is also applied to flip-flop 2D5B. This flip-flop is initially placed in the-clear state (RQST-P low/RQST-N high) by the pull-up circuit consisting of inverters 2C6A and 2C6B. The flip-flop remains in the clear state until LOAD-P is produced when the operator makes a beam request. This sets the flip-flop, producing a high-level RQST-P. ADDRCMPR-N and LOAD-P now produce REQUEST-P in the following manner. ADDRCMPR-N is applied to the preset (S) input of flip-flop 2D7A. This preset level sets the flip-flop to produce a high-level ADDR-P. RQST-P (previously generated by LOAD-P) and ADDR-P are simultaneously applied to NAND gate 2D4A to produce RQST B-N. Inverter 2D4B inverts RQST B-N to produce REQUEST-P. REQUEST-P is again inverted by inverter 2F5A to produce a low level REQUEST-N. This signal is coupled to the position scanner and hence to the computer.

3. Shift Register Clear. At the same time REQUEST-N is being produced, SR CLEAR-N is being produced to clear the shift register. This is accomplished as follows. ADDR-P, produced in FF2D7A, and ADDRESS-P produce a low-level ADD CLR-N in NAND gate 2E7D. ADD CLR-N is applied to NOR gate 2E6A producing SR CLEAR-P. SR CLEAR-P is inverted by inverter 2E6B and applied to the preclear inputs of shift registers SR1D6B, SR1DSA and SR1D4A. The

shift register is now cleared of any high level signals and is prepared to receive serial or parallel data.

4. Beam/Band Select. At this time (Phase B cycle), the position scanner produces a low-level DATA-N signal. This signal is inverted by inverter 2E3A and applied to NAND gate 2E3C. The high-level DATA-P signal, in unison with high-level REGNABL-P and a high-level REQUEST-P produce PRESET-N. PRESET-N is inverted by inverter 2E2A and the resultant high-level is applied to the shift register. The high-level PRESETP parallel loads the beam request data word stored in the beam request storage register (bits 10, 11, 12, 13, and 14) and receiver in use (NABLE 1) (bit 9) in the shift register.

NOTE

A high-level NABLE 1-P requests rf signals to receiver 1. A low-level NABLE 1-P requests rf signals to receiver 2.

PRESET is generated in the following manner. REQUEST-P partially enables NAND gate 2E2C when generated by ADDR-P and RQST-P. Gate 2E3C is further enabled by a high-level REGNABL-P. This signal is produced by a NAND gate flip-flop consisting of NAND gates 2F3A and 2F3C. This flip-flop is gated to the set state (REGNABL-P is high, REGNABL-N is low) by ADDRESS-P. The flip-flop remains in this state, thereby enabling NAND gate 2E3C until a CLOCK B-N pulse clears the flip-flop (REGNABL-P is low, REGNABL-N is high). The clock pulse of interest is used to serially shift the beam request data word to the computer. The position scanner now provides seven clock pulses (CLOCK-N). The first CLOCK-N pulse gates the flip-flop comprised of NAND gates 2F3A and 2F3C to the clear state. In this state, the flip-flop produces a high-level REGNABL-N. The high-level REGNABL-N partially enables NAND gates 2E3B and 2F3B. The low-level REGNABL-P returns/PRESET-N to a high level.

5. Serial Out Data. The CLOCK-N pulses serially shift the data out of the bsu/biu shift register to the position scanner through NAND gate 2E5A. NAND gate 2E5A is enabled by the high-level REQUEST-P and NHBTSDOT-P. NHBTSDOT-P is produced by a flip-flop comprised of NAND gates 2F6A and 2E6C. Initially, this flip-flop is placed in the clear state by PWR UP CLR-N when power is applied to the bsu/biu. The flip-flop remains in this state and NHBTSDOT-P is a low level until PRESET-N is produced. PRESET-N, generated by 2E3C, sets the flip-flop producing a high-level NHBTSDOT-P. While high, the serial out NAND gate 2E5A is enabled and the serial data (SEROUT) is gated through. Upon receipt of the CLEAR B-N signal the flip-flop returns to the clear state. In this state the serial out NAND gate 2E5A is again inhibited.

6. Clock Return. The seven clock pulses are returned to the position scanner through NAND gate 2F5B to load the 7-bit beam request word. This NAND gate is enabled by the high-level REQUEST-P signal.

7. Removal of Request. After producing the seven clock pulses used to shift the 7-bit beam select word, the position scanner produces a CLEAR-N pulse. This pulse gates NOR gate 2E6A, to again produce SR CLEAR-N. SR CLEAR-N again clears the shift register. CLEAR-P is applied to flip-flop 2D7A; the trailing edge clears the flip-flop. The resultant high-level ADDR-N triggers one-shot 2C7B to produce a 0.2-microsecond DELAY-P pulse. DELAY-P and a high-level INHBTRST-N produced by a flip-flop comprised of NAND gates 2F1A and 2E1A, produce low-level reset

request (RSTRQST-N) signal. RSTRQST-N is gated through NOR Gate 2C6B and inverted by inverter 2C5A to clear request storage flip-flop 2D5B. The resultant low-level RQST-P signal produces a low-level REQUEST-P, removing the request from the output of the bsu/biu.

8. Rf Signal Path. The computer analyzes the beam request signal to determine the request azimuth, radio frequency band, and receiver. Binary control signals are formulated and coupled to the switch matrix to select the desired rf path. The switch matrix makes the appropriate switch closures to couple the requested beam rf signal to the receiver associated with the requesting bsu/biu. The rf signal is analyzed by the olm&t circuitry for amplitude characteristics. If the rf signal is found to be satisfactory, a 14-bit message is formulated by the computer to identify the azimuth band and receiver. The azimuth is identified by a 10-bit BCD word, divided into three parts. The first part is 4 bits representing the units digit, the second part is 4 bits representing the tens digit, and the third part is 2 bits representing the hundreds digit. The band is identified by a 2-bit word, 00 representing band A, 01 representing band B, and 10 representing band C. The receiver is identified by a single bit with a high level representing receiver number 1 and a low level representing receiver number 2. If the computer is unable to provide a satisfactory rf path, a fault lamp and blanking signal are output to the bsu/biu. A code of 11 in the band data position is used to blank the azimuth and band display; a 1 bit in the fault data position lights the FAULT lamp; and the azimuth bits in the 14 bit message are disregarded. The 14 binary bits representing these items and the appropriate bsu/biu address is coupled from the computer to the position scanner during phases A and B.

9. Azimuth and Band Storage. The address of the bsu/biu is stored by the position scanner. The position scanner during phase D produces nine clock pulses to serially shift the 9-bit address word to the shift register of the bsu/biu. Immediately following the loading of the address word, the ADDRESS-N signal is coupled to the bsu/biu. The resulting ADDRCMPR-N signal sets flip-flop 2D7A producing ADDR-P and ADDR-N. The high-level ADDR-P and ADDRESS-P signals gate NAND gate 2E7D producing ADD CLR-N. The low-level ADD CLR-N gates NOR gate 2E6A producing SR CLEAR-N. SR CLEAR-N is inverted by inverter 2E6B to clear the shift register. The data word is then loaded into the bsu/biu shift register by 14 clock pulses (CLOCK-N) during phase E. At the conclusion of the serial shift, DATA-N pulse is produced. This DATA-N pulse is instrumental in parallel loading the display storage register with the azimuth and band BCD words stored in the shift register. These words are stored in receiver 1 display storage register consisting of SR1F2A, SR1E2A, and SR1D2A; or in the receiver 2 display storage register consisting of SR1F2B, SR1E2B, and SR1C2A. The particular display storage register to be used is selected by STROBE 1 (receiver 1) and STROBE 2 (receiver 2). These signals are produced upon receipt of DATA-N as follows.

(a) A high- or low-level A-RCVR signal (high-receiver 2, low-receiver 1) is stored in SR1D6B. This signal is applied directly to NAND gate 2E3B and, after being inverted by inverter 2G3A, the signal is applied to NAND gate 2F3B. The high or low state of A-RCVR as received from the computer therefore determines which of these two NAND gates (2E3B or 2F3B) are enabled to produce a strobe pulse (STROBE 1 or STROBE 2). The timing of the strobe pulse is determined by DATA B-P, ADDR-P, and REGNABL-N. REGNABL-N is produced by a NAND gate flip-flop consisting of NAND gates 2F3A and 2F3C. The flip-flop is set by ADDRESS B-N, producing a low level REGNABL-N, when the position scanner conducted the address search. At the same time, an ADDRCMPR-N signal is also produced. This signal sets flip-flop

2D7A to produce ADDR-P. Immediately after serially shifting in the 14-bit azimuth/band message, the position scanner produces DATA-N. DATA-P, ADDR-P, and REGNABL-N are applied to NAND gates 2F3B and 2E3B. The gate enabled by high-level A-RCVR signal now produces a low-level output, either STROBE 1-N or STROBE 2-N. These strobe signals are applied to the display storage register to parallel load the azimuth and band data words and to NOR gate 2F2A. (b) The low-level STROBE signal is inverted in NOR gate 2F2A and again in inverter 2F2B. The resultant low-level STROBE OR-N sets NAND gate toggle 2FlA. The resultant low-level INHBTRST-N is applied to NAND gate 2C6A. This low-level signal inhibits the NAND gate, thereby preventing the generation of RSTRQST-N. The RSTRQST-N signal would normally be generated if it were not for this signal by the ADDR-N signal. The inhibiting of RSTRQST-N inhibits the generation of an unwanted REQUEST-N signal.

10. Clearing Bsu/Biu Registers. The position scanner at this point produces a CLEAR-N pulse. The pulse, as before, gates NOR gate 2E6A to produce SR CLEAR. This signal is again applied to the shift register to clear all data from the register.

11. Azimuth and Band Display. Display of the AZIMUTH and BAND in use is controlled by RCVR 1 (S21) and RCVR 2 (S22) switches, Pressing one of these switches triggers the flip-flop consisting of NAND gates 2H7A and 2G7A to the set or clear state. The resultant NABLE i-P from the set state enables the receiver 2 display storage register. In an enabled state, the data stored is displayed in the AZIMUTH and BAND indicators. NABLE i-N enables receiver 1 display storage register for displaying receiver 1 AZIMUTH and BAND.

12. Fault Display and Message. The FAULT switch (S23) is used to notify the Console, Operation and Maintenance OJ-263/FLR-9(V) (somc) of a problem at the intercept position. Pressing FAULT switch produces a 5-bit beam select BCD word, FAULT-N and OR-N. The OR-P and beam select BCD words perform identical functions are previously described. These functions allow the computer to receive the fault word. Upon receipt of this word, a computer routine is called up to provide a message to the system control group tty. The message notifies the somc operator of the fault and the bsu/biu which is experiencing the problem with the following printout: Fault @ OPER XXX RCVR Y. The FAULT-N signal sets the flip-flop comprised of 2C3D and 2B3A producing FLT-N. FLT-N enables NOR gate 2B2A which provides drive power to light the FAULT lamp (DS23). Flip-flop is comprised of 2C3D and 2B3A, remains in the set state until a BEAM SELECT switch is again pressed. At this time FAULT-N is high. This signal, in unison with the LOAD pulse, gates NAND gate 2B4A. The resultant low-level output returns the toggle comprised of 2C3D and 2B3A to the clear state. The resultant high-level FLT-N extinguishes the FAULT lamp.

13. Blanking. If for any reason the path verification test fails, an unassigned BEAM SELECT switch is pressed, an invalid address is used with a bsu/biu, or the bsu/biu fails, the BEAM/AZIMUTH display is blanked when a beam is requested. The blanking occurs as a result of a blanking message from the operating computer. This blanking signal contains a logic in both the A-BAND 1-P and A-BAND 2-P signal levels. These two highs are stored and inverted in storage register A2U1. The two resultant high level outputs are inverted in NAND Gate 1G1A to clear the display fiber optic circuits.

14. No Beam Display and Message. The NO BEAM switch (S24) is pressed when an rf path to a receiver is no longer required. Pressing NO BEAM switch produces a 5-bit select word and signals NO BEAM-N and OR-N. The OR-n

signal and beam select word perform identical functions as previously explained. These functions allow the computer to receive the no beam word. Upon receipt of the word the computer provides binary signals to the switch matrix to connect the receiver to a 75 ohm load or make the switch points available for other uses. The NO BEAM-N signal produced by S24 sets flip-flop comprised of 2C3A and 2C3G producing NBM-N level. NBM-N is inverted by Inverter 2C2A to provide drive power to light the NO BEAM lamp (DS24). The flip-flop comprised of 2C3A and 2C3G remains in the set state until a BEAM SELECT switch is pressed. At this time NO BEAM-N is high. This high-level signal in unison with LOAD-P returns the flip-flop comprised of 2C3A and 2C3G to the clear state.

c. Mechanical Circuits. No mechanical devices are used in the bsu/biu.

4-6. Special Project Bsu/Biu Detailed Description.

a. Principles of Operation. (See figure 4-4.)

1. Interrogation. The position scanner continuously interrogates the special project bsu/biu by sequentially shifting a 9-bit serial binary address word (SERIN) to the address recognition circuits of each bsu/biu. The address word is followed by an address-validate (ADDRESS) pulse which allows the addressed position to return a beam service request (REQUEST) if one has been requested by the operator since the last scan of the position scanner.

2. Request. A request is produced only when the operator presses the BEAM SET switch. The BEAM SET switch signal enables storage and gating circuits to produce the REQUEST-N pulse when the respective special project bsu/biu are addressed.

3. Addressing. Each special project bsu/biu has an address which is determined by the setting of three switches. Signals from these switches are routed to address recognition logic. Address signals are routed to the special project bsu/biu shift register from the position scanner on the SERIN-N line, along with CLOCK-N signal. After shift register loading, If the loading was address, the ADDRESS-N signal goes low. The ADDRESS-N signal partially enables address recognition logic, which also receives address signals from the shift register. If shift register content has an address, and if that address is the same as the special project bsu/ biu, address recognition logic produces one of two ADDRCMPR-N signals. The ADDRCMPR-N signal activates storage and gating logic, producing the REQUEST-N signal. When the position scanner receives the REQUEST-N signal, it routes a CLEAR-N signal to all special project bsu/biu. The CLEAR-N signal and ADDRESS-N signal, together, enable storage and gating circuits to clear the shift register contents and continue the operating sequence.

4. Transmission. After shift register contents are cleared, PRESET-N signal causes loading of data bits 8 through 14 from a storage register into the shift register. Content of this storage register amounts to selected antenna azimuth, as encoded by diode gating. The storage register is divided into three sections, one section for each of three possible digits in the azimuth angle. The units, tens, and hundreds sections of the storage register are selectively enabled by a multiplier decoder which counts the number of digits entered. After the shift register is loaded (and ADDRESS-N and CLEAR-N signals are removed), each CLOCK-N pulse causes shift register contents to move over one space. Output

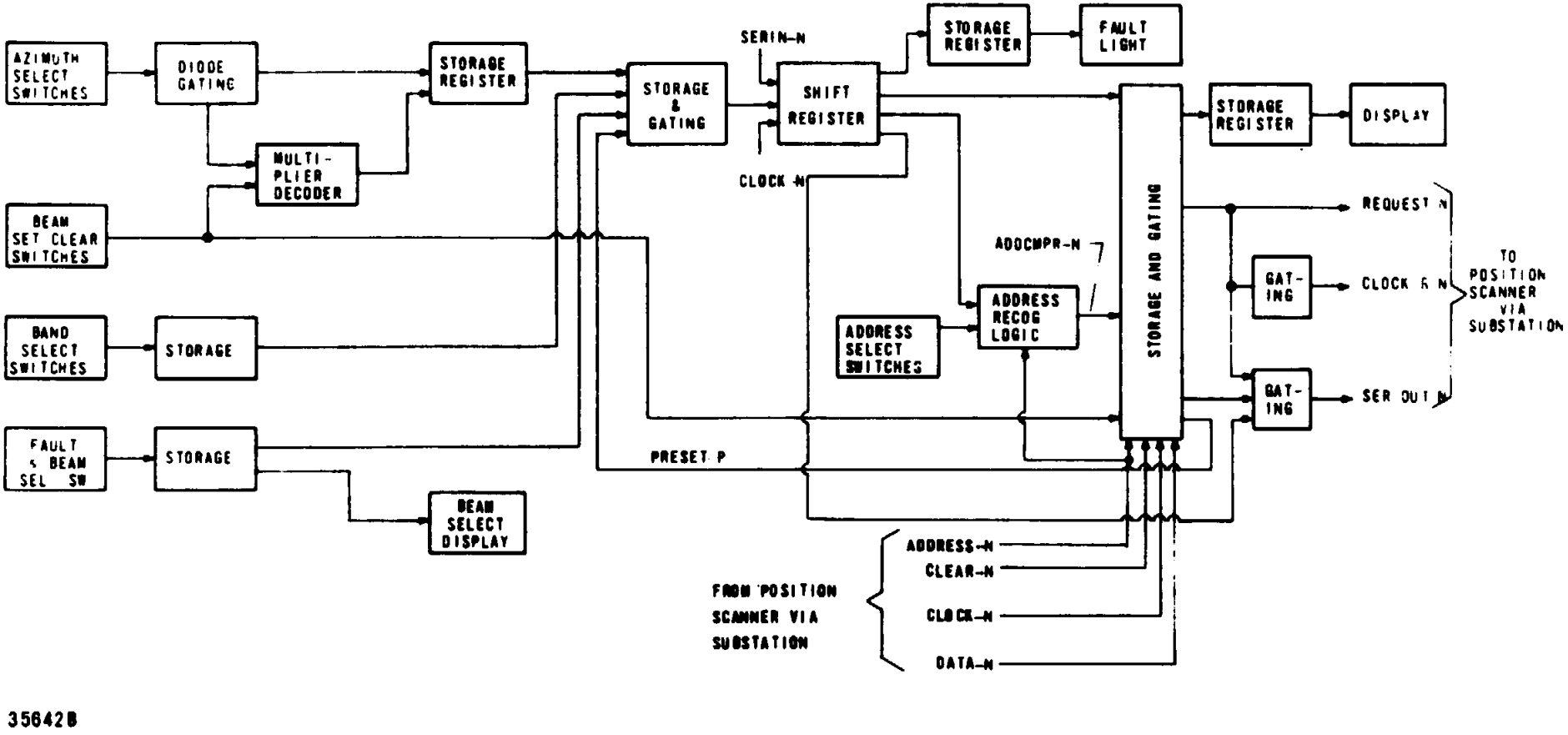


Figure 4-4. Special Project Bsu/Biu Block Diagram

from the last shift register stage is then routed out through a gating circuit to the position scanner as SEROUT-N signal. After transfer of the seven shift register data bits, the position scanner sends a second group of address bits followed by ADDRESS-N signal. As before, the address bits are loaded into the shift register adding binary 1 to the previously used address. Shift register output then activates the second-address portion of the address recognition logic. Address recognition logic consequently issues a second ADDRCMPR-N signal. The second ADDRCMPR-N signal causes storage and gating circuits to produce a second PRESET-N signal. As before, the position scanner issues a CLEAR-N signal to clear address bits from the shift register. The second PRESET-N signal causes the loading of antenna azimuth bits 5 through 7, both band bits, and both beam fault bits into the shift register through storage and gating circuits. Switches that initiate these signals actually control storage flip-flops and a storage register, so their commands are present even though their action is momentary. Contents of the loaded shift register are again moved out to the position scanner by CLOCK-N signal. During both transmissions of shift register contents (during the REQUEST-N signal), clock pulses are routed out through a gating circuit as CLOCKR-N signal.

5. Reception. After the special project bsu/biu sends the contents of its shift register the second time, the position scanner again sends address bits followed by ADDRESS-N and CLEAR-N signals, as before. After clearing the shift register, the position scanner sends a data word on the SERIN-N line. The data word is shifted into the shift register by the CLOCK-N signal. After the data word is loaded, the position scanner sends the DATA-N signal. The DATA-N signal causes storage and gating circuits to enable loading of shift register contents into a storage register for display of computer-selected antenna azimuth and band. Output from the same storage and gating circuits also enables storage circuits to pass fault signal to the front panel display.

b. Electronic Circuits. (See figure 7-5.)

1. Address Recognition. The position scanner polls a special project bsu/ biu by issuing an address word and an ADDRESS-N signal. The address word enters the shift register consisting of 2H7A, 2F7A, and 2E7A serially on the SERIN-N line. It is shifted into the shift register by CLOCK-N signal. The SERIN-N line is terminated by resistors R5 and R6; its signals are inverted by inverter 2G8A. The clock signal line is terminated by resistors R7 and R8; signal is inverted by inverter 2F8A. Shift register outputs are routed to exclusive-OR gates 2H5A through 2F5D. The second input to each of these exclusive-OR gates is biased so that a particular pattern (address) from the shift register is necessary to activate all gate outputs. The second inputs to exclusive-OR gates 2G5C, 2F5A, and 2F5B are biased through three switches (56, S7, and S8). The switches select the logic-level bias for each input, providing manual control of individual special project bsu/biu address. Outputs from exclusive-OR gates 2H5A through 2F5B are routed to NAND gate 2G4A. When all of its inputs go high, the main address is valid and NAND gate output goes low. The NAND gate output is inverted by inverter 2G3A and routed to NAND gates 2G2A and 2G2B, partially enabling them. The ADDRESS-N signal line is terminated by resistors R4 and R16; its signal is inverted by inverter 2H3A to become ADDRESS-P signal. This signal is present if shift register content is actually an address. The ADDRESS-P signal is routed to NAND gates 2G2A and 2G2B, further enabling them. Each special project bsu/biu has two addresses; the two bits that distinguish these are from exclusive-OR gates which activate either NAND gate 2G2A or 2G2B. The activated NAND gate output goes low and is called ADDRCMPRI-N or ADDRCMPR2-N.

2. Response to Address. Special project bsu/biu response to address recognition occurs after BEAM SET switch (A21S16) is pressed. Pressing this switch puts a pulse across resistors R11 and R28. The logic high from these resistors is inverted by inverter 3D6B and routed to the clock input of J-K flip-flop 3D4B. At the end of the pulse on its trigger input, J-K flip-flop 3D4B changes state when ADDCMPRI-N is low, producing the RQST-P signal. When ADDR-P signal is present, NAND gate 3D3B passes RQST-P signal, which is reinverted by inverter 3D2A. Output from 3D2A is distributed to the position scanner through NAND gate 3E5B as REQUEST-N signal (signifying that updating is required) and to NAND gates 3D2B and 3C2A. These NAND gates are enabled by REQUEST P and REGNABL-P signals. The REGNABL-P signal comes from the flip-flop comprised of NAND gates 3G3A and 3F3A. This flip-flop produces the REGNABL signal when position scanner CLOCK-N signal is high and ADDRESS-N signal is low (one-half clock period after ADDRESS-N comes from the position scanner). Therefore PRESET 1-N is produced by NAND gate 3D2B one-half clock period after the bsu/biu address is recognized and PRESET 2-N is produced by NAND gate 3C2A each time the bsu/biu address recognition is followed by a data word (signified by the DATA pulse).

3. Antenna Azimuth Switches. Antenna azimuth is selected by use of numeric switches located on A21. Every time a switch is used, it applies a logic pulse (logic high) to one of the inverters in 1F7A and 1D7A, driving the diode matrix consisting of 1G6A and 1E6A. Low output from the respective inverter holds the left diode-matrix line low. Every time this line called OR-N goes low, it triggers single-shot 1A7A. The single-shot output goes low, inhibiting NAND gates 1B6B through iA6B for the time determined by the single-shot timing network. Every time the diode matrix left line goes low, J-K flip-flop 1B7A is also triggered. And every other time J-K flip-flop 1B7A is triggered, its output triggers J-K flip-flop 1B6A. Thus, flip-flops 1B7A and 1B6A comprise a three-counter. The three-counter outputs are routed to NAND gates 1B6B through 1B6B. At the end of the single-shot output pulse, one of these NAND gates is activated by both of the count (CNTn-N or CNTn-P) signals at its input. Output from these NAND gates is inverted by inverters 1B5A through 1A5B; each inverted output is routed to the load input of one of the three storage register stages (1G4A through 1D4A). Each NAND gate/inverter/storage register stage accommodates one of the three digits necessary to define an antenna azimuth angle. The remainder of the diode matrix provides binary coded decimal (BCD) output for each switch. The BCD outputs are inverted and loaded into the enabled storage register, hundreds digit, tens digit, and then units digit. If the numbers are entered incorrectly, the three-counter and the storage register can be reset. Reset is accomplished when the BEAM CLEAR switch (A21S8) is pressed. The consequent logic high signal from resistors R12 and R29 is inverted by inverters 1B8A and 1B8B, Output from inverter 188A clears the three-counter flip-flops 1B7A and 1B6A. Output from inverter 188B clears flip-flop contents and, after inversion by inverter 1H5A, clears the content of each shift register stage.

4. Beam Select Fault, and Band Switches. The switches used to select the type of beam, the band, and to indicate a fault are momentary-contact. When they (A17 through A20 and S2 through S4) are pressed, they apply ground to the biased input of an associated NAND gate. This NAND gate comprises part of a flip-flop. Grounding the NAND gate input sets the flip-flop, providing storage and inhibiting response to contact bounce. For beam select and fault switches, flip-flop low output is routed to a lamp driver, causing that lamp driver to ground the floating terminal of an associated indicator lamp. The low outputs from each of these flip-flops are tied to the inputs of the other flip-flops in the group,

preventing selection of more than one at a time. Flip-flop outputs associated with the sector, and omni beam switches and the fault switch are routed to NAND gates, called BM+FLT2-P and BM+FLT1-P, respectively, are routed to AND gates in 1F2A for selective loading into the shift register. The status of the BM+FLT1-P and BM+FLT2-P signals Is unique for each switch in the group. If both are low, monitor beam was selected; if both are high, the fault switch is pressed. If only BM+FLT1-P is high, omni beam is selected. And, finally, if only BM+FLT2-P is high, a sector beam is selected. The three band select switches control two flip-flops which produce unique outputs on two lines. The flip-flops, consisting of NAND gates 1C3A/1C3B and 1B3A/1B3B, are set individually if band B or C is selected. If band A is selected, both flip-flops are cleared. If the beam clear switch is used, both of these flip-flops and the beam/fault select flip-flops are cleared. And also, the band select flip-flops clear each other when bands B and C are selected. Band select flip-flop outputs are routed to AND gates in 1G2A for selective loading into the shift register.

5. Transmission. The PRESET-N signals, derived as described in subparagraph 4-6.b.2, are routed from NAND gates 302B and 3C2A to NAND gate 1B1B. Only one PRESETn-N signal is present at a time; PRESET 1-N occurs in response to the first address. The inverted PRESET 1-N signal is applied to a row of AND gates in 1G2A, 1F2A, 1E2A, and 1D2A. This signal enables those AND gates to pass azimuth angle data bits 8 through 14. Output from each of these AND gates corresponds to azimuth angle data input. The AND gate outputs are inverted by OR gates, then passed on to inputs of shift register stages 2F7A and 2E7A. Shift register stages accept these inputs due to the PRESET (not numbered) signal. The PRESET signal comes from NAND gate 1B18 whenever PRESET 1-N or PRESET 2-N signal is present. The second address activates PRESET 2-N signal. After inversion, this signal enables a second group of AND gates to pass the remaining azimuth angle data bits, the two BAND bits, and the BM+FLTn-P bits through the OR gates to the shift register. For either address, PRESET-P signal is inverted by inverter 2D7A to set the flip-flop consisting of NAND gates 3F60 and 3E5A. The consequently high NHBTSDAT-P signal, along with REQUEST-P signal, partially enables NAND gate 3E5C. The output from the last stage of the shift register BIT 15-N, controls NAND gate 3E5C. As the shift register contents are moved into the last stage by CLOCK-N signal, they are inverted and routed out to the position scanner by NAND gate 3E5C and called SEROUT-N. At the end of each transmission, the position scanner sends the CLEAR-N signal. The line for this signal is terminated by resistors R1 and R13. The signal is inverted and reinverted by inverters 3F8A and 3F6C. Inverted CLEAR-N signal triggers J-K flip-flop 3D7B, clearing it (because of the biased J-K inputs), and also activating NOR gate 3F6B. Output from 3F6B is inverted by inverter 3F5A to become SR CLEAR-N signal. The SR CLEAR-N signal clears the contents of the shift register (2E7A-2H7A). The CLEAR B-N signal from inverter 3F6C clears the flip-flop consisting of NAND gates 3F6D and 3E5A. Clearing this flip-flop removes NHBTSDAT-P signal, inhibiting transmission of data through NAND gate 3E5C. The ADDR-N signal from J-K flip-flop 3D7B goes high when this cleared. The high signal triggers single-shot 3B7A; the single-shot produces a pulse (called DELAY-P) with length determined by a resistor and capacitor. The DELAY-P pulse activates NAND gate 385A, producing DELCOMP-N signal which is inverted and reinverted by NOR gate 385B and inverter 3B4A. The resulting signal, called RQSTCLR-N, clears J-K flip-flop 3D48. Clearing this flip-flop removes the REQUEST-N signals, CLOCK R-N output, and both PRESETn-N signals. The other flip-flop 3D7B output, called ADDR-P, is grounded. This has two effects.

(a) It enables NAND gate 3F6A to respond to the next ADDRESS-P signal. (High output from this NAND gate is ignored by gate 3F6B until its other input goes high at the end of the CLEAR-N signal.)

(b) It disables NAND gate 3F3B which inhibits STROBE-N signal and inhibits operation of the flip-flop consisting of NAND gates 3F2A and 3E2A.

6. Display. After the position scanner has sent the CLEAR-N signal, it again sends the first address word and the ADDRESS-N signal followed by a data word and a signal called DATA-N. When DATA-N signal arrives, the shift register (2H7A, 2F7A and 2E7A) is loaded with 12 bits of data that represent actual selected antenna azimuth angle and frequency band. The DATA-N signal line is terminated by resistors R5 and R17; its signal is inverted by inverter 3F3C, then applied to NAND gate 3F3B. Also applied to this NAND gate are REGNABL-N and ADDR-P signals. Presence of all three signals activates NAND gate 3F3B to produce the STROBE-N signal and set the flip-flop comprising NAND gates 3F2A and 3E2A. The consequent high flip-flop output, called INHBTRST-N, enables NAND gate 3B5A to (ultimately) clear J-K flip-flop 3D4A and remove the REQUEST-N signal. The STROBE-N signal is routed to a storage register consisting of 2F2A, 2E2A and 2D2A. The STROBE signal causes the storage register to load and hold the 12 data bit output from the shift register. Storage register output controls the numbers displayed on indicators DS1 through DS4. Another CLEAR-N signal is sent after the DATA-N signal to clear the shift register and prepare for the next cycle.

7. FAULT Display and Blanking. The faults displayed in the FAULT lamp and the blank BEAM/AZIMUTH display are identical to the circuits described in paragraphs 4-5.b.13 and 4-5.b.14.

c. Mechanical Circuits. No mechanical devices are used in the special project bsu/biu.

4-7. Substation.

a. Principles of Operation. (See figure 4-5.)

1. General. The substation is a buffer for signals between the position scanner and bsu/biu at each intercept group position. In buffering the signals, an interface between the position scanner and eight bsu/biu is provided. In this manner the interface allows one position scanner input/output to service eight bsu/biu. A protection circuit is provided so that when a substation power supply output is less than 2.5 volt dc, the interfacing signals in the position scanner are inhibited.

2. Signal Amplifiers. Position scanner input signals are buffered by two cascade amplifiers. The buffered signal is coupled to eight identical distribution amplifiers. Distribution amplifiers provide signal distribution to eight bsu/biu. input signals from the bsu/biu are buffered by two cascade amplifiers on each signal line. The output of each signal line buffer amplifier is coupled through a common bus line to two output cascade amplifiers. The output amplifiers couple the signal to the position scanner.

3. Substation Inhibit Circuit. (See figure 7-6.) If pin J1-b (STROBE-P signal) in a substation is grounded, the interface circuits in the position scanner are enabled to allow signals from the bsu/biu units connected to that substation. This ground is broken if the substation/position scanner cable is disconnected.

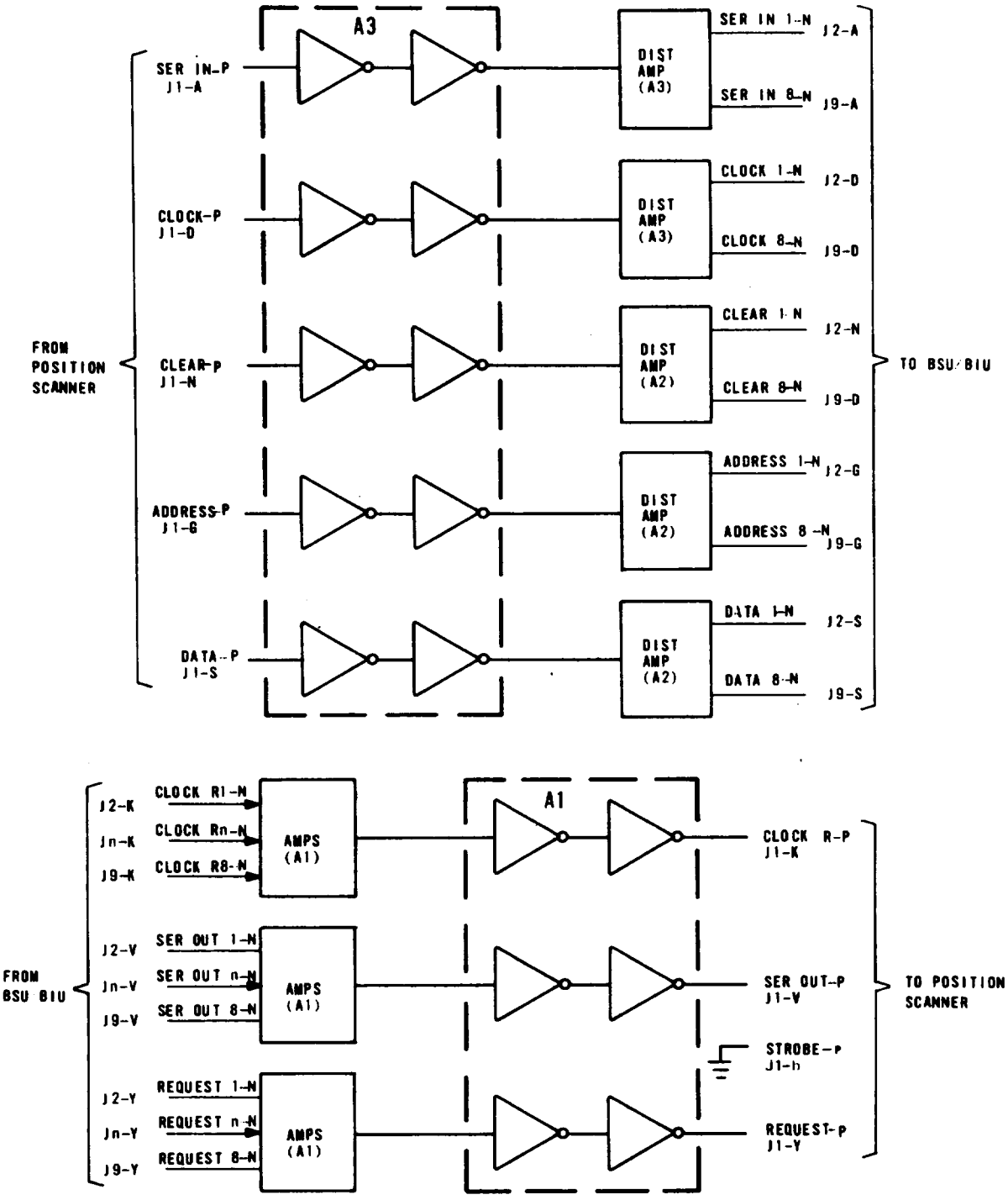


Figure 4-5. Substation Block Diagram

It is also broken by the contacts of relay K1 if the output of the substation +5 volts dc power supply is less than 2.5 volt dc. Should the cable be disconnected or the power supply output fail due to malfunction or power interruption, the position scanner interface circuits are disabled and computer interrogation of and communication with the bsu/biu's associated with the affected substation is prevented.

b. Electronic Circuits. (See figure 7-6.) The substation is an interface between the position scanner and the bsu/biu. Distribution amplifiers in each substation distribute the input/output signals of the position scanner to/from eight bsu/biu. The five command signals from the position scanner (SERIN-N, CLOCK-N, CLEAR-N, ADDRESS-N, and DATA-N) are applied to distribution amplifiers. Forty distribution amplifiers, eight for each of the five inputs, distribute the signals to eight output jacks (J2 through J9). The pin connections on these eight jacks are identical, i.e., SERIN-N is connected to pin A on all output jacks. Cables from the output jacks distribute the signals to eight bsu/biu. Three signals from the bsu/biu (RQST-N, SEROUTN, and CLOCK R-N) are applied to collection amplifiers. These signals are amplified by the common collection amplifier and coupled to the position scanner.

4-8. Position Scanner.

a. Principles of Operation. (See figure 4-6.)

1. General. The position scanner detects beam service requests from the bsu/biu positions and sends these requests on to the computer for action. It also accepts the beam service verification word from the computer and sends this data on to the bsu/biu for display. The position scanner operates asynchronously from the computer, and interrupts the computer at level 13 each time a beam service request is detected. When a beam service verification word is to be returned, the computer addresses the position scanner, and waits for an ACKNOWLEDGE signal from the position scanner before transferring the data to the position scanner for transfer to the bsu/biu.

2. Timing. The position scanner operates at a basic frequency of 1 MHz. The timing is derived from a self-contained 1-MHz oscillator. Intermediate frequencies of 1, 10, and 50 kHz are derived by frequency dividers. The 100-microsecond period required for the scan of each position is divided into five phases by a phase generator. A complete scan cycle (512 bsu/biu address positions) is repeated each 51.2 milliseconds. A slightly longer cycle time may be required during receipt of a beam service request.

3. Address. The scan address is derived from a nine-stage scan counter which furnishes as many as 512 discrete position addresses. The positions are scanned sequentially by shifting a serial binary address word out to the address recognition circuits of each bsu/biu. The address word is followed by an address validate pulse (V-pulse), then a data-pulse (D-pulse). The V-pulse is converted to a bsu/biu ADD-N pulse (called ADDRESS) which allows the addressed bsu/biu to detect its own address. ADDRESS allows the addressed position to return a beam service request (REQUEST-N) if one has been requested by the operator at that position since the last scan.

4. Request. Upon receipt of REQUEST-P signal, the position scanner sends a serial burst of seven clock pulses on the clock line. These are used by the addressed bsu/biu to shift the beam request message onto the SEROUT-N line. These pulses are also turned around by the bsu/biu and returned to the position scanner as CLOCKR-N pulses.

The CLOCKR-N pulses shift the 7-bit returned message into a storage register. After the last clock pulse, the position scanner sends a CLEAR-N pulse (C-pulse) to the bsu/biu and generates a computer interrupt. The scan address counter is inhibited until the computer acknowledges the interrupt and strobes the 16-bit word containing the position address and the beam and receiver information from the bsu/biu. The computer acknowledgment releases the scan address counter inhibit, and normal scanning is resumed.

5. Beam Request Reply. When the computer has completed action on a beam service request, it addresses the position scanner and returns an address word and a verification word to the position scanner. The address word contains the address of the bsu/biu from which the beam service request originated. The data word contains the fault, receiver, band and azimuth information. The address word is transferred first and stored in a 9-bit latch by the position scanner. The verification word is transferred next and stored in a 14-bit latch by the position scanner. The 9-bit address word is placed on the SERIN line concurrent with nine clock pulses on the clock line. The clock pulses are followed by an ADDRESS-N signal (V-pulse) which allows the addressed bsu/biu to validate the address. The 14-bit verification word is then placed on the bsu/biu SERIN line concurrent with 14 clock pulses on the clock line. The clock pulses shift the serial word out of the position scanner and into the bsu/biu storage register. The last clock pulse is followed by DATA-N signal (D-pulse) on the data line, then a CLEAR-N signal (C-pulse) on the clear line. The D-pulse allows the bsu/biu to store the received word and the clear pulse resets the bsu/biu control circuits. In each scan period, 40 microseconds are reserved for transfer of these two words; therefore, the scan cycle is not interrupted or delayed.

6. Data Transfer. The serial address and message transfers between the position scanner and the bsu/biu positions are accomplished by controlling the generation of clock pulses which clock this data out of and into the respective units. Bursts of 7, 9, and 14 clock pulses are used for this action. The generation of these clock bursts is controlled by presetting a downcounter to a count equal to the number of desired clocks, then decrementing until the count equals zero. The borrow output of the counter is used to inhibit the generation of clock pulses once the desired number has been reached. The desired count configuration for the preset is placed at the downcounter input during the phase preceding the phase in which it is to be used. The count is loaded into the downcounter by a strobe pulse at the beginning of the using phase. In this manner, the input and output registers are synchronized by using the same effective pulse for the transfer out and the transfer in.

7. Phase Timing. (Refer to figure 7-7.) The 100-microsecond scan period for each position is divided into 20-microsecond phases by a phase generator. These phase signals are used throughout the timing and control circuits to control the interrogate, reply, and idle modes of the position scanner.

(a) During phase A, the scanner address counter is incremented to the address of the next bsu/biu position to be scanned and this address is placed in the output shift register. The interrogate flag is set to prepare for the interrogation scan that is accomplished in the next phase.

(b) At the beginning of phase B, the interrogate flag is set, a clock counter is preset to allow generation of the nine clock pulses required for the interrogation, and the current scan address is in the shift-register. During the first

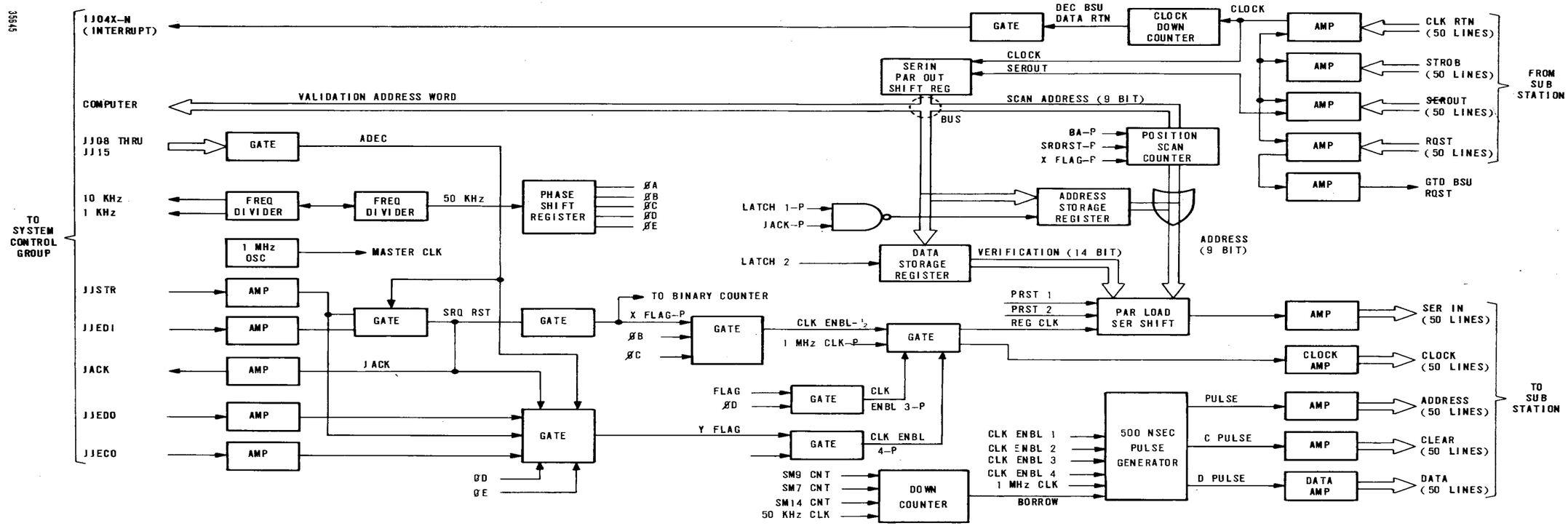


Figure 4-6. Position Scanner Block Diagram

nine clock periods of the phase, the clock pulses are placed on the clock line and the 9-bit address is placed on the SERIN line. During the tenth clock time, a V-pulse is generated, and during the eleventh clock period, a D-pulse is generated. Following the D-pulse, the scanner is prepared to detect a RQST-N signal from the bsu/biu position. If no RQST-N is present, the scanner reverts to the idle mode for phase C. If a RQST-N is detected, a flip-flop is set. This inhibits the scan counter and sets up the timing and control conditions for the reply mode for phase C.

NOTE

Only the six least significant bits of the reply message are used in the normal bsu/biu. Seven bits are used in the special project bsu/biu.

(c) During phase C, a burst of seven clock pulses is generated on the clock line. These clocks are returned by the bsu/biu as CLOCK R-N pulses, concurrent with the 7-bit reply message from the bsu/biu. This message is shifted into the shift register. At the eighth clock time, a C-pulse is sent on the clear line. When the last SEROUT-N line data bit has been shifted into the shift register, an interrupt (1J04X) to the computer is generated. A JJED1 pulse from the computer acknowledges the interrupt and transfers the parallel 16-bit message to the computer. The JJED1 pulse also resets the RQST flip-flop, thus releasing the scan counter inhibit.

(d) During phases D and E the position scanner is in the reply mode. These two phases are reserved for the transfer of beam service verification to the requesting bsu/biu. If a beam service request verification message has been received during phases A, B, or C, the transfer to the bsu/biu begins in phase D. During the first nine clock periods, a burst of pulses on the clock line transfers the bsu/biu position address on the SERIN-N line. The position address furnished by the computer is stored in a 9-bit latch prior to the transfer. During the tenth clock period, a V-pulse is sent on the address line. The 14-bit verification message is then transferred from storage to the shift register during phase E.

(e) During the first 14 clock periods of phase E, a 14-bit clock burst on the clock line transfers the 14-bit verification message on the SERIN-N line. A D-pulse is sent during the fifteenth clock period, followed by a C-pulse on the clear line (during the sixteenth clock period). This terminates the data transfer; at the completion of phase E, the scanning continues, uninterrupted.

b. Electronic Circuits. (See figure 7-7.).

1. Timing. The basic timing for the position scanner is furnished by 1-MHz oscillator 1E7A. The oscillator output is a 1.0 microsecond symmetrical square wave. This signal is counted down to 10 kHz in two series decade frequency dividers, 1G5A and 1G5B. The output is split at 1G4B and routed to the watchdog timer circuits in the system control group. The 10-kHz signal is further divided by decade frequency divider 1G4A to furnish a 1-millisecond interrupt signal to the computer. An optional operating frequency of 500 kHz is also available from flip-flop 1E5A which halves the frequency of the master clock. The 1.35-millisecond single-shot 1F7A provides a MSTR RST pulse each time power is applied to clear all control circuits.

2. Scan Timing. Each scan period is 100 microseconds in duration and consists of five equal 20-microsecond phases. These phases are designated ΦA, ΦB, ΦC, ΦD, and ΦE from counter registers 1C5A and 1C5C. The 50-kHz input to the phase counter is derived from a decade frequency division of the master clock at 1C7A, which is halved by

flip-flop 106A. Refer to figure 7-7 for the time, frequency, and relationship of the phase signals.

3. Phase A. During phase A, the scan address counter is incremented, to the address of the next bsu/biu to be scanned; the reply flag (Y-flag) is cleared; a count of nine is preset into the downcounter which controls the generation of the register and counter clocks; and the new scan address is transferred to the serial output shift register. Phase A is initiated by the leading edge of the positive 20-microsecond phase A signal at 1C5A. This signal is inverted at inverter 2F8A producing (SM9 CNT INT)-N. The negative leading edge of (SM9CNT INT)-N triggers single-shot 2F7C to form the (A START)-N signal, resets flip-flop 4F5A/4G4A, inhibits (SM14 CNT)-N, and conditions the inputs of downcounter 11B4B through the diode network at 11B6A. The (A START)-N pulse clears the Y-Flag flip-flop 3D4A. The negative transition of the set output of single-shot 2F7C (A START)-P clocks flip-flop 2F6A, delaying the gate output of 2G5A approximately 1 microsecond after the beginning of phase A. The (PRST1A)-P signal output from this gate is inverted by NOR gates 8G6A and 8G6B to form (PRST 1)-P. This is the preset signal which loads the bsu/biu address from the scan address counter into the data shift registers (11F6A, 11F5A, 11F4A, 11F3A). The (PRST1A)P signal is inverted by inverter 2F4A to form (M9STRB INT)-N which loads the preset count of nine into downcounter 11B4B.

4. Phase B. At the beginning of phase B, the data shift register contains the 9-bit address of the bsu/biu to be scanned. In addition the clock control downcounter has been loaded with a count of nine. During phase B, the serial address is shifted to the bsu/biu on the SERIN line and nine clock pulses are concurrently placed on the clock line, followed by a V-pulse at the tenth clock time on the address line, and a D-pulse during the eleventh clock time on the data line. The 20-microsecond phase B signal (D PULSE 1)-P is gated with X FLAG-P at gate 8F6A. The resultant (D PULSE INT)-N signal is gated with (PHASE-B)-P and X FLAG-P at NAND gate 3G7A producing (REG/CNTR RST 1)-P. This signal is gated through NOR gate 8B5A to clear the data/address shift register consisting of SR11F6A, SR11F5A, 11F4A, and 11F3A. The phase B signal (D PULSE-INT) is gated with XFLAG-P at gate 3G7D and inverted at inverter 3G7E to form (CLK ENBLI)-P. This inverted signal enables gate 3E6A and 4B3B triggers single-shot 8E6B, and partially enables the V pulse and D pulse gates. Armed gate 3E6A awaits the bsu/biu request (GTD BSU RQST)-P during phase B to form (R PULSE)-N. This signal clears flip-flop 3F5B/3E5A, resets shift register 17D5A/17C5A, and resets binary counter 17B6A. The high-level output of single-shot 8E6B sets flip-flop 8D5A while the low-level output sets flip-flop 8D4B. The high-level output of 8D5A partially enables the bsu clock gate 8C3A and register clock gate 8D3A. The counter clock gate (8D3A) passes ten 1-MHz clock signals during the time the set output of flip-flop 8D4B is high. Flip-flop 8D4B is preset to the set state by the leading edge of the low-level output of single-shot 8E6B 1 microsecond after the beginning of phase B; it is cleared by BORROW-N output of the downcounter after nine clock pulses. Flip-flop 8D5A is used in the same manner to enable the bsu and REG clock gates. The register clocks at the output of gate 8C3D are inhibited during portions of phase C. During the tenth clock pulse period, (V PULSE 1)-P and (V PULSE 2)-P are generated at gates 4G2C and 4G2D. The pulse generation is dependent upon the BORROW-N input to gate 4D7A and the (CLK ENBL 1)-N signal at 4G2A. The BORROW-N input clocks flip-flop 4D7B which enables 4D6A to pass one master clock pulse. Gate circuits 4D6B and 4D6C and flip-flop 4D4A clear flip-flop 4D7B and sets flip-flop 4C7A at the end of the tenth clock pulse. Flip-flop 4C7A arms gate 4C6A to pass the eleventh master clock pulse. This pulse becomes the 0-pulse at gates 4B2C and

4B2D. Gates 4C5B and 4C5A and flip-flop 4C4A clear flip-flop 4C7A at the end of the eleventh clock period. The controlling signal (CLK ENdL-1)-P allows generation of the V and D-pulses during phase B. Following generation of the D-pulse, the circuits are armed for the receipt of a bsu/biu . request pulse from the addressed bsu/biu. If a request for service is not present at the bsu/biu, a RQST pulse is not generated and significant action does not occur during the remainder of phase B. Receipt of a RQST pulse following the D-pulse produces signal GTD BSU RQST-P at gate 14B6A; produces (R-Pulse)-14 at gate 3E6A; and sets the request flip-flop at 3F5B/3E5A. The negative leading edge transition of (R PULSE-N signal resets the 7-bit shift register (17D5A, 17C5A) and binary counter 17B6A. The shift register is cleared in preparation for receipt of the request message during phase C. The request message is a 7-bit word for the bsu/biu and special project bsu/biu. At this same time, the counter is cleared in preparation for counting the CLK R pulses during phase C.

5. Phase C. The positive leading edge transition of signal (PHASE C)-P is inverted at gate 3F5A, where the negative leading edge transition triggers single-shot 3F4A. The low-level 100-nanosecond output (M7STRB)-N loads the count of seven into downcounter 11B4B. The trailing edge positive transition of single-shot 3F4A in conjunction with(PHASE C-P clocks flip-flop 3F3A to the set state. While set, the Q-N output (SM9CNT)-N of flip-flop 3F3A is inverted by gate 3F3B, producing a high-level (CLK ENBL 2)-P signal. (SM 9 CNT)-N enables the preset count of nine at the inputs of downcounter 11B4B which is preset into the counter at the beginning of phase D. The (CLK ENBL 2)-P signal enables the generation of the seven bsu clocks and eight cnt clock pulses in the same manner as that previously described for phase B. However, the V and D pulses are inhibited and C PULSE 1-P and C PULSE 2-P are generated by BORROW-N after the eighth master clock. The seven bsu clock pulses are returned from the bsu/biu as CLOCK R-N pulses only if a RQST signal is received during phase B. The returned CLOCK R pulses produce shift clock pulses at shift register 17D5A, 17C5A, shifting the SEROUT-N data from the bsu/biu position into the shift register. The CLOCK R-N pulses are also counted in serial counter 17B6A. The seven-count detect gate 17B6B is conditioned after receipt of the seventh CLOCK R pulse, and triggers single-shot 17B6C. The output pulse (DEC BSU DATA RTN)-N clears flip-flop 2G7B/2F7A, partially enabling gate 2G7A, generating an interrupt to the computer via the high-level JO4X signal, and causing X FLAG-P signal to go to a low level. In addition, the low input to gate 2F7B enables gates 2D6A, 2C6A, 2B6A, and inhibits the output gate of the scan address counters 2D5A and 2D4A. The position scanner interrupts the computer at level 13. Therefore, the interrupt produced by signal JO4X is acknowledged in the (A-JJEDI)-P signal. The EDI signal from the computer, with a concurrent strobe pulse (AJJSTR)-P, produces (GTDASEDI)-N pulse at gate 2H6A. This pulse generates XJACK-P signal via gates 3C3B and 3C3C. The XJACK-P signal is the position scanner acknowledgment to the computer. GTD ASEDI-P sets flip-flop 3B5A. The Q output with AJJEDI-P produces a delayed EDI (SRQ RST) at 3B5B. This signal sets X FLAG-P 2F7A and partially enables the scan address counter. The 16-bit word containing the bsu/biu address and seven bits of data is transferred to the computer in parallel via the differential line drivers. Transfer of this 16-bit word is enabled by AFFEDI-P signal through gates 17H4A through 17B4A. The scan address counter inhibit is released by JJEDI-N. The circuit conditions are now prepared for the beginning of phase D.

6. Reply Mode. Phase D and Phase E are reserved for the reply mode. The reply mode is denoted by signal Y-flag and is active when a computer reply is received during the preceding phase A, B, or C portion of the scan. If no reply from the computer is received, the position scanner assumes the idle mode during phases D and E, and no significant action takes place. The computer reply starts with ECO command and a concurrent strobe signal. If the scanner is in phases A, B, or C, the ECO command (AJJECO)-P conditions gate 3C5C, producing a low-level (LATCH 1 OUT ENBL)-N pulse. This pulse with XJACK-P stores the address word from the computer in the 9-bit register (lE2A, 1D2A, 1C2A). The low output of gate 3C5C is inverted at gate 3C5B, and with the concurrent STR, conditions gate 3C4A, thus setting flip-flop 3D4A, and producing XJACK-P signal via 3C3A, 3C3B, and 3C3C. The XJACK-P is the acknowledge pulse which tells the computer that the address word on the input lines has been accepted and stored. Upon receipt of this acknowledgment, the computer responds with the second word of the reply, consisting of an EDO pulse (AJJEDO)-P and a concurrent strobe pulse. The EDO pulse conditions gate 3C5A, producing (LATCH 2 OUT ENBL)-N. This signal pulse and the concurrent strobe pulse produce the acknowledge pulse XJACK-P. The acknowledge pulse and the (LATCH 2 OUT ENBL)-N pulse combine at gate 1OB6A to transfer the 14-bit reply word into storage registers (1OC6A, 1OC4A, 1OC3A, 1OC2A). If the computer attempts to transfer a reply during phases D and E, the acknowledgment and transfer is inhibited at gate 3C6A. The computer continues the attempt until the position scanner leaves phase E and begins phase A of the 'next scan. This releases the inhibit and the transfer takes place as previously described. The address and data words are then set to the appropriate bsu/biu during the next phase D and E cycle.

7. Phase D. (Reply Cycle). Signal YFLAG-P at a high level denotes that reply words are stored in their respective storage registers and awaiting transfer to the appropriate bsu/biu. The presence of Y-flag signal at the beginning of phase D (PHASE D)-P produces a low level at the output of gate 4G6C, triggering single-shot 4G5A. The Q-N pulse (M 9 STRB)-N becomes (CNTR STRB)-N at gates 8G6E and 8G5A. (CNTR STRB)-N presets a count of nine into the clock control counter 11B4B. This allows generation of the nine clock pulses which transfer the bsu/biu address word. Single-shot 4G5A set-side output Q-P sets flip-flop 4G4A and produces (PRST 1B)-P signal. (PRST 1B)-P becomes (PRST 1)-P at gates 8G6A and 8G6B. The (PRST 1)-P signal presets the 9-bit address word into output shift register 11F6A, 11F5A, 11F4A, and 11F3A. The low-level 1-N output of flip-flop 4G4A conditions gate 4G4B, thus enabling the register and counter clock with a high-level (CLK ENBL-3)-P signal. The nine register clocks and ten counter clock pulses enable the shifting of the 9-bit address word out serially on the SERIN-N line. The BORROW-N signal after the ninth clock triggers the control circuit flip-flop 4D7B.. This allows the generation of V-pulse via gate 4D6A, 4D6B, 4D6C and 4G2A. The V-pulse occurs at the tenth counter clock pulse. It is used by the addressed bsu/biu to validate the address, and prepare to receive the 14-bit data word. The low-level (V PULSE)-N conditions gate 4F6A, producing (REG/CNTR RST3)-P signal which resets the shift register in preparation for transfer of the second word.

8. Phase E. The presence of YFLAG-P at the beginning of phase E is detected at gate 4E6A, where the leading edge negative transition of the gate output triggers single-shot 4E6B. The 1-N output of the single-shot (M14 STRB)-N presets the counter control downcounter with a count of 14. The 1-P output of the single-shot 4E6B strobes the 14-bit data word from the 14-bit latch into the shift register with the high-level (PRST 2)-P signal at 11F6A. The negative

transition of the trailing edge of signal (PRST 2)-P sets flip-flop 4F5A. The low-level 1-N output of this flip-flop conditions gate 4E4A, producing a high-level (CLK ENBL4)-P signal. This signal also partially arms gates 4C3A and 4C3B for subsequent generation of a D and C-pulse. The 14 register and counter clock pulses are produced and place 14 clock pulses on the clock line. Concurrently, they shift the 14-bit data message from the shift register to the bsu/biu on the SERIN-N line. After the fourteenth clock pulse, BORROW-N signal from the clock control downcounter clocks flip-flop 4D7B. This subsequently produces a D-pulse at clock 15 time, and a C-pulse at clock 16 time. The C-pulse clears the bsu/biu circuits and resets the output shift register and the downcounter through gates 4E6C and 8B5A.

4-9. Power Supply, PP-6813/FLR-9(V).

a. General. Each type bsu/biu and the substation use Power Supply, PP-6813/ FLR-9(V). The following circuit description defines this power supply.

b. Principles of Operation. (See figure 4-7.) The 120-volt ac input is reduced by a stepdown transformer. The stepped down ac voltage is rectified and filtered by two separate circuits. The load rectifier and filter supplies 5 ±0.5 volts dc at 4 ±0.4 amperes to the series regulator. The internal rectifier and filter supplies ±0.5 volts dc to bias the internal reference zener diode and to provide power for the internal driver and control transistors. The internal rectifier and filter supplies dc voltage and current to the series regulator which is connected in series with the output. The voltage across the series regulator varies as the input voltage, load, and other conditions change to maintain a set output voltage. The series regulator is controlled by the regulator control circuit error voltage. The error voltage is generated by the regulator control circuit which compares two inputs, a reference voltage from a zener diode and the output voltage. The difference between these two voltages is sensed and an error signal is produced. The error signal is amplified and used to control

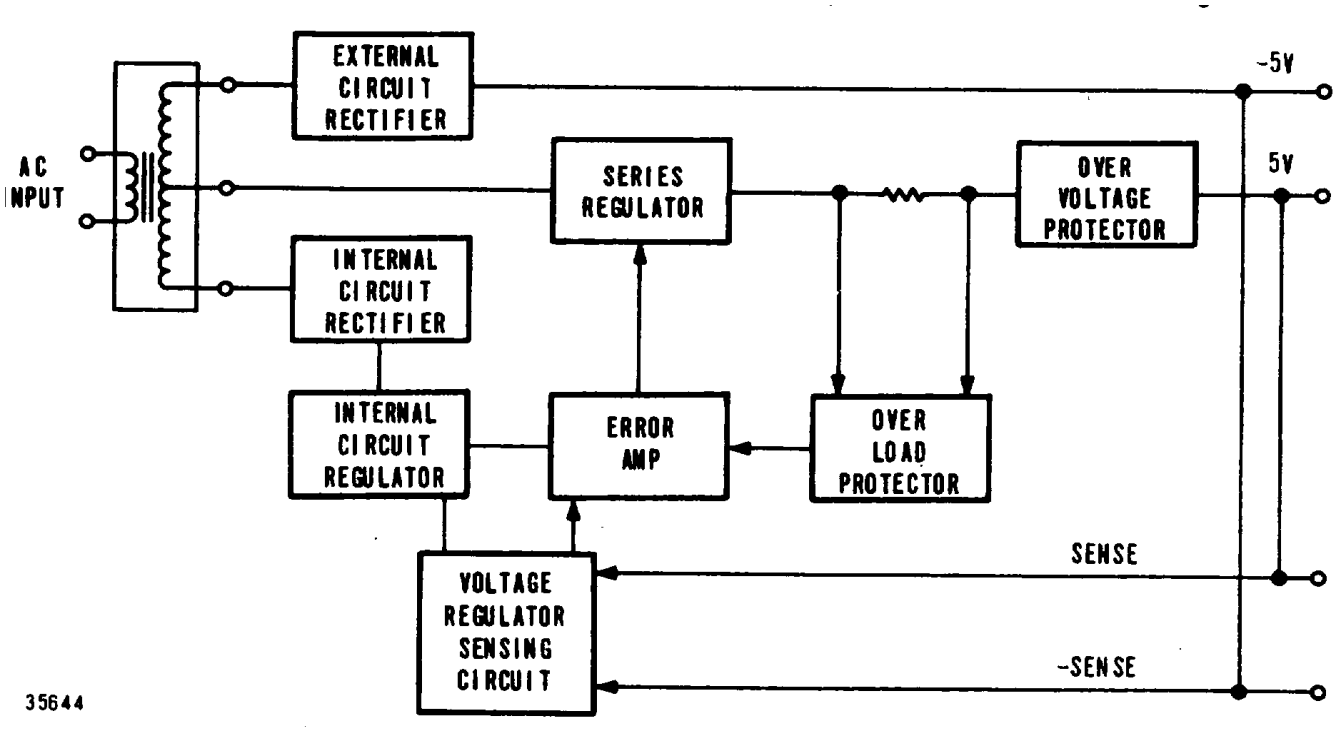


Figure 4-7. Power Supply PP-6813/FLR-9(V) Block Diagram

the voltage across the series regulator. The overvoltage circuit samples the output voltage of the series regulator. When this voltage exceeds a preset value (+6 volts dc) the overload circuit is saturated. As a result, the regulator control circuit and the series regulator are cut off to cause the output voltage to decrease. The overvoltage circuit is a SCR crowbar type. In the circuit a reference voltage is compared to the output voltage. The resultant error voltage drives the SCR into conduction when a preset value is obtained. The SCR, while conducting, shorts (crowbars) the output.

c. Electronic Circuits. (See figure 7-8.)

1. Rectifier. The 110-volt ac input voltage is stepped down by transformer T1. The stepped-down voltage is applied to rectifiers CR1, CR2, CR3, and CR4. CR1 and CR2 form a full-wave rectifier which supplies current to the external load through series regulator Q8. CR1, CR2, CR3, and CR4 form a bridge-type rectifier which supplies current to internal circuits. The external supply (CR1 and CR2) is filtered by capacitors C1 and C2. The internal supply is filtered by C6.

2. Series Regulator. The negative dc line is coupled directly to the negative output. The positive dc is connected through the series regulator transistor Q8 results in regulator action against line and load changes.

3. Voltage Regulator. A sample of the output voltage from R15 and R16 is compared by the differential amplifier Q3 and Q4 with a reference voltage derived from a zener reference element and divider R2 and R3. When Q4 conducts, the base drive is reduced to Q6, Q7, and Q8. Controlling the base drive of Q8 provides regulator action.

4. Internal Circuit Regulator. CR5, a zener diode is the reference voltage for two open loop constant current sources Q1 with R4, and Q2 with R8. Q1 and R4, maintain a constant bias current through the reference element CR6 and divider R2 and R3. Q2 and R8 provide constant current for Q4 and driver transistor Q6.

5. Overload Protection. The load current is sensed by the voltage drop across R18 and R21. The overload transistor Q5 conducts and reduces the base current of Q6 which provides current limiting. At short circuit, the loss of output voltage and the bias level set by divider R13 and R14 cause the short circuit current to be limited to a value less than rated current.

6. Overvoltage Protection. Overvoltage protection is afforded by the overvoltage assembly. This protection is accomplished through the high current capacity of CR5. CR5 conduction is controlled by an error signal generated by differential amplifier consisting of Q1 and Q2. The error signal is generated by comparing the load voltage to a reference voltage produced by CR1. When the load voltage rises more than 2 volts (adjustable by R7), the error signal drives Q3 into saturation. The saturation current of Q3 drives CR5 into conduction. While conducting, CR5 places a very low impedance across the power supply output, thus reducing the load voltage.

4-10. Detailed Integrated Circuit Description. (See tables 4-1 through 4-5.)

The paragraphs that follow contain descriptions of integrated circuits used on custom-made printed-circuit cards for Countermeasures Receiving Sets AN/FLR-9(V7) and AN/FLR-9(V8) Intercept Group. Tables 4-1 through 4-4 list the

Table 4-1. Bsu/Biu Circuit Cards

Circuit ; Card Reference Designator	Circuit Card Part Number	Circuit Card Reference Designator	Circuit Card Part Number
A1	3300-44056-1	A3	3300-44058-1
A2	3300-44057-1	A4	3300-44059-1

Table 4-2. Special Project Bsu/Biu Circuit Cards

Circuit Card Reference Designator	Circuit Card Part Number	Circuit Card Reference Number	Circuit Card Part Designator
A1	3300-44023-1	A9	3300-44082-1
A2	3300-44118-1	A10	3300-44123-1
A3	3300-44124-1	A11	3300-44131-1
A4	3300-44119-1	A12	3300-46015-1
A5	3300-44120-1	A13	3300-44125-1
A6	3300-46012-1	A14	3300-44126-1
A7	3300-44121-1	A15	3300-44127-1
A8	3300-44122-1		

Table 4-3. Bsu/Biu Substation Circuit Cards

Circuit Card Reference Designator	Circuit Card Part Number
A1	3300-44060-1
A2	3300-44061-1
A3	3300-44062-1

Table 4-4. Position Scanner Circuit Cards

Circuit Card Reference Designator	Circuit Card Part Number	Circuit Card Reference Designator	Circuit Card Part Number
A101	3300-46149-1	A202	3300-46021-1
A102, A114	3300-46007-1	A203	3300-46022-1
A103, A115	3300-46008-1	A205	3300-46025-1
A104	3300-46009-1	A206	3300-46023-1
A105	3300-46010	A207	3300-46024-1
A106	3300-46011-1	A208	3300-46029-1
A107, A111, A116	3300-46012	A109	3300-46025-1
A108	3300-46013	A210	3300-46026-1
A109	3300-46146	A211 through A226	3300-46027-1
A110	3300-46015	A301 through A326	3300-46028-1
A112	3300-46147	A409 through A411	3300-46027-1
A113	3300-46150-1	A414 through A416	3300-46027-1
A117	3300-46148-1	A412	3300-44070-1
A118	3300-46017-1	A417 through A424	3300-46028-1
A119	3300-46018-1	A204	Empty slots
A120	3300-46019-1	A401 through A408,	Empty slots
A121 through A126	3300-44070-1	A413, A425	Empty slots
A201	3300-46020-1	and A426	Empty slots

Table 4-5. Intercept Group Integrated Circuit Complement

	PCB No. 3300-				
IC No.	**44056**	**44057**	**44058**	**44059**	**44060**
3300-44028-1*	U1/U2/U3				
SN7400		U8	U2/5/6/7/9		
SN7401					
SN7402					
SN7404			U3/4/8	U10/12	U4/5/7/9
SN7405					U3/6/8/10
SN7410			U10	U9	
SN7420			U12		
SN7430	U11				
SN7440		U9/10	U1		
SN7450					
SN7472			U11	U5	
SN7486	U9/10			U11	
SN7490					
SN7494					
SN7496	U6/7/8				
SN74107					
SN74121					
SN74193				U6/7	
DM8551N	U4/5	U1 - U6			
MC4024P					
HC840P					
MH0017CN				U1/2/3/4	
U7B961459X					
U5B961559X					U1/2
N8271B					
	44120	44121	44122	44123	44124
3300-44028-1*					
SN7400					
SN7401					
SN7402					

*3300-44028-1 is a diode matrix defined in paragraph 4-10.w.

Table 4-5. Intercept Group Integrated Circuit Complement (Continued)

	PCB No. 3300-				
IC No.	**44120**	**44121**	**44122**	**44123**	**44124**
SN7404 SN7405 SN7410 SN7420 SN7430 SN7440 SN7450 SN7472 SN7486 SN7490 SN7494 SN7496 SN74107 SN74121 SN74193 DM8551N MC4024P MC840P NHOO17CN U7B961459X U7B961559X N82718	U1/2/3	U1 - U4	U1 - U4	U4 U1-U3	U1 - U3
	44125	44126	46007	46008	46009
3300-44028-1* SN7400 SN7402 SN7404 SN7405 SN7410	U1/U2	U1/2/3	U1 - U4		

Table 4-5. Intercept Group Integrated Circuit complement (Continued)

	PCB No. 3300-				
IC No.	**44125**	**44126**	**46007**	**46008**	**46009**
SN7420 SN7430 SN7420 SN7430 SN7440 SN7450 SN7472 SN7486 SN7490 SN7494 SN7496 SN74107 SN74121 SN74193 DM8551N MC4024P HC840P NHO017CN U7B961459X U7B961559X N82718	U3/U4	U4		U1 - U4	U1 - U4
	46010	46011	46012	46013	46015
3300-44028-1* SN7400 SN7401 SN7402 SN7404 SN7405 SN7410 SN7420 SN7430			U1 - U4	U1 - U4	U1 - U4

Table 4-5. Intercept Group Integrated Circuit Complement (Continued)

	PCB No. 3300-				
IC No.	**46010**	**46011**	**46012**	**46013**	**46015**
SN7440 SN7450 SN7472 SN7486 SN7490 SN7494 SN7496 SN74107 SN74121 SN74193 DM8551N MC4024P MC840P NHOO17CN U7B961459X U7B961559X N8271B	U1 - U4	U1 - U4			
	46017	46018	46019	46020	46021
3300-44028-1 * SN7400 SN7401 SN7402 SN7404 SN7405 SN7410 SN7420 SN7430 SN7440 SN7450	U1 - U4		U3/4		U1 - U4

Table 4-5. Intercept Group Integrated Circuit Complement (Continued)

	PCB No. 3300-				
IC No.	**46017**	**46018**	**46019**	**46020**	**46021**
SN7472					
SN7486			U1/2		
SN7490					
SN7494					
SN71496					
SN74107					
SN74121					
SN74193				U4	
DM8551N		U1 - U4		U1/2/3	
MC4025P					
MC840P					
NHO017CN					
U71B961459X					
U7B961559X					
N8271B					
	44061	44062	44082	44118	44119
3300-44028-1 *					
SN7400					
SN7401					
SN7402					
SN7404					
SN7405					
SN7410					
SN7410					
SN7420					
SN7430					
SN7440	U1 - U12	U1 - U8			
SN7450					
SN7472					
SN7486					

Table 4-5. Intercept Group Integrated Circuit Complement (Continued)

	PCB No. 3300-				
IC No.	**44061**	**44062**	**44082**	**44118**	**44119**
SN7490					
SN7494					
SN7496			U1/2/3		
SN74107					U1/3
SN7421					U2/4
SN74193					
DM8551N					
MC4024P					
MC840P					
NHO017CN					
U7B961459X					
U7B961559X		U9/10/11			
N8271B					
	46022	46023	46024	46027	46028
3300-44028-1 *					
SN7400					
SN7401					
SN7402					
SN7404		U1/2/3			
SN7405					
SN7410					
SN7420					
SN7430					
SN7440					
SN7450					
SN7472					
SN7486					
SN7490	U1/2/3				
SN7494			U1/2/3		

Table 4-5. Intercept Group Integrated Circuit Complement (Continued)

	PCB No. 3300-				
IC No.	**46022**	**46023**	**46024**	**46027**	**46028**
SN7496					
SN74107					
SN74121					
SN74193					
DM8551N					
MC4024P					
MC840P		U4			
NH0017CN					
U7B961459X					U1 - U4
U7B961559X				U1 - U4	
N8271B					
	46029	46146	46149	46150	
3300-44028-1*					
SN7400					
SN7401			U1		
SN7402					
SN7404			U3		
SN7405					
SN7410					
SN7420					
SN7430					
SN7440					

Table 4-5. Intercept Group Integrated Circuit Complement (Continued)

	PCB No. 3300-			
IC No.	**46029**	**46146**	**46149**	**46150**
SN7450				
SN7472				U1/3
SN7486				
SN7490				
SN7494				
SN7496				
SN74107				U2/4
SN74121		U2/4	U4	
SN74193				
DM8551N				
MC4024P			U2	
MC840P				
NH0017CN				
U78961459X				
U7B961559X				
N8271B				

circuit card part numbers used in the intercept group equipment. Table 4-5 provides a cross reference between circuit part numbers and applicable manufacturer's integrated circuit type numbers.

a. SN7400 Quadruple Two-Input Positive NAND Gate. (See figure 4-8.) The SN7400 Integrated circuit contains four identical positive logic two-input NAND gates. The output of each such gate is at logic low only when both of its Inputs are at logic high. If either input is low, the output is high. Connections are shown in figure 4-8.

b. SN7401 Quadruple Two-Input Positive NAND Gate. (See figure 4-8.) The SN7401 integrated circuit contains four identical positive logic two-input NAND gates with open-collector outputs. The output of each such gate is at logic low only when both of its inputs are at logic high. If either input is low, the output is an open circuit. Connections are shown in figure 4-8.

c. SN7402 Quadruple Two-Input Positive NOR Gate. (See figure 4-8.) The SN7402 integrated circuit contains four identical positive logic two-input NOR gates. The output of each such gate is at logic low when either input, or both inputs, are at logic high. If both inputs are low, output is high. Connections are shown In figure 4-8.

d. SN7404 Hex Inverter. (See figure 4-8.) The SN7404 integrated circuit contains six identical signal Inverters. The output logic level for each inverter is opposite its respective input logic level. Connections are shown in figure 4-8.

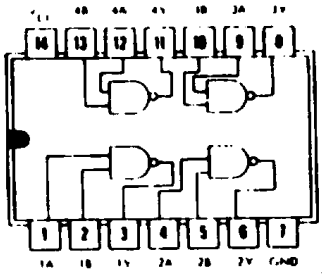
e. SN7405 Hex Inverter. (See figure 4-8.) The SN7405 integrated circuit contains six identical signal inverters with open-collector outputs. The output of each inverter is at logic low when its input is at logic high. When an inverter input is at logic low, its output is an open circuit. Connections are shown in figure 4-8.

f. SN7410 Triple Three-Input Positive NAND Gate. (See figure 4-8.) The SN7410 integrated circuit contains three identical three-input positive-logic NAND gates. The output of each such gate is at logic low only when all of its inputs are at logic high. If any input is low, the output is high. Connections are shown In figure 4-8.

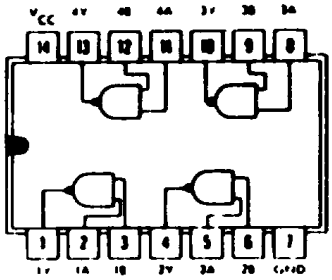
g. SN7420 Dual Four-Input Positive NAND Gate. (See figure 4-8.) The SN7420 integrated circuit contains two Identical four-input positive-logic NAND gates. The output of each such gate is at logic low only when all of its inputs are at logic high. If any input is low, the output is high. Connections are shown in figure 4-8.

h. SN7430 Eight-input Positive NAND Gate. (See figure 4-8.) The SN7430 integrated circuit contains an eight-Input positive-logic NAND gate. The output of this gate is at logic low only when all eight inputs are at logic high. If any input is low, the output is high. Connections are shown in figure 4-8.

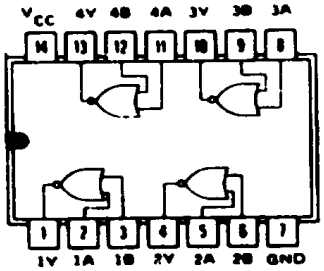
i. SN7440 Dual Four-Input NAND Buffer. (See figure 4-9.) The SN7440 Integrated circuit contains two identical four-input positive logic NAND gates designed to serve as buffers. The output of each such gate is at logic low only when all of its inputs are at logic high. If any input is low, the output is high. Each gate has a normalized fanout (drive) capability of 30 as compared to 10 for non-buffer type integrated circuits. Connections are shown in figure 4-9.



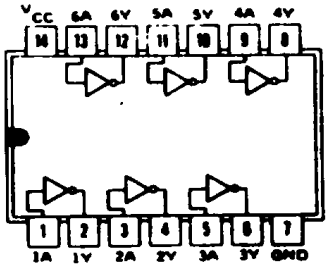
a. (SN7400)



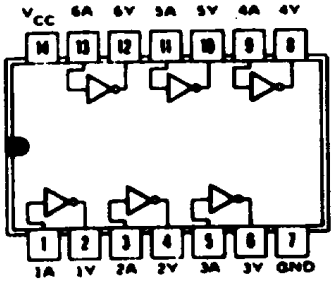
b. (SN7401)



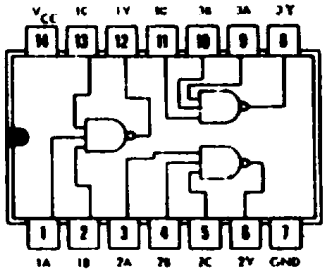
c. (SN7402)



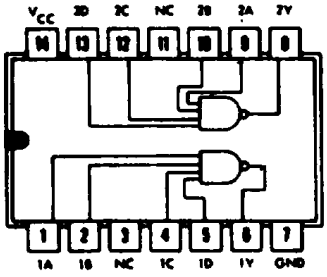
d. (SN7404)



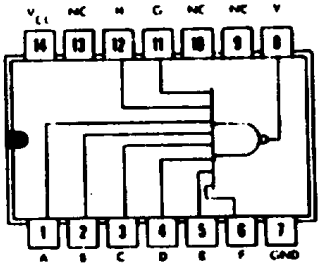
e. (SN7405)



f. (SN7410)



g. (SN7420)



h. (SN7430)

Figure 4-8. Integrated Circuit Connections

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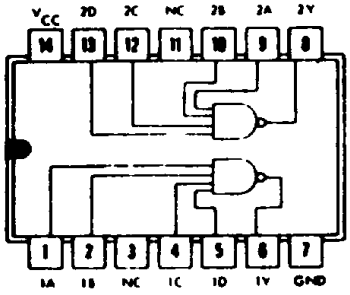
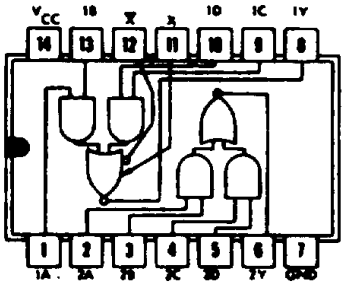
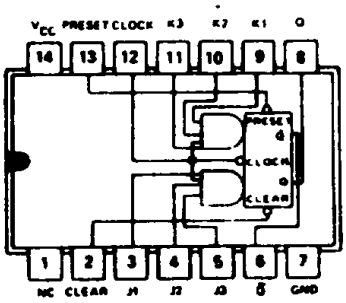


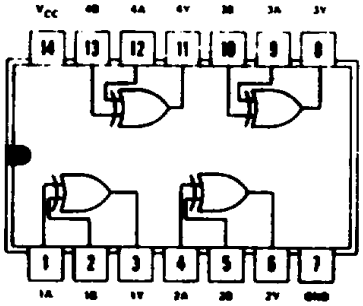
a. (SN7440)



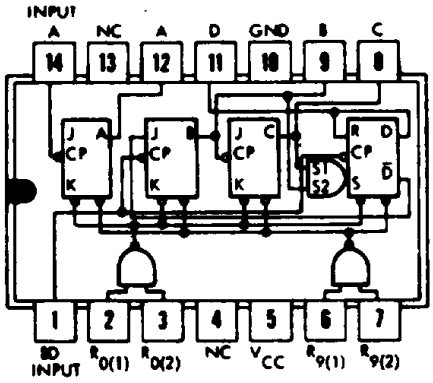
b. (SN7450)



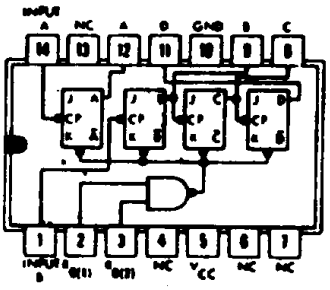
c. (SN7472)



d. (SN7486)



e. (SN7490)



f. (SN7493)

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Figure 4-9. Integrated Circuit Connections

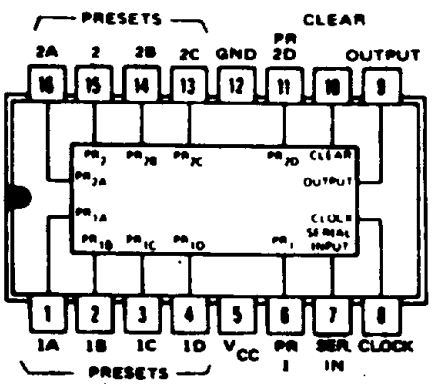
j. SN7450 Expandable Dual Two-Wide Two-input AND-OR-INVERT Gate. (See figure 4-9.) The SN7450 integrated circuit contains two nearly identical circuits. Refer to figure 4-9 for details, Each circuit consists of a two-input NOR gate driven by two two-input AND gates. The output of either NOR gate is at logic low when both Inputs to one or both of its AND gates are high. If one or both Inputs to both AND gates are at logic low, NOR gate output is at logic high. In addition, one of the NOR gates is provided with an expansion input. Output of the NOR gate is at the same logic level as the expansion input logic level.

k. SN7472 J-K Master-Slave Flip-Flop. (See figure 4-9.) The SN7472 integrated circuit contains a J-K type flip-flop. Connections are shown in figure 4-9. Two asynchronous inputs are provided, preset and clear. Either of these inputs causes response independent of the clock input. A low-level preset input sets the Q output to logic high. A low-level clear input sets Q output to logic high. The preset and clear inputs have priority over the J-K inputs. The J-K Inputs are transferred to the output after the clock pulse voltage reaches a particular level, if preset and clear inputs are both high. The J and three K inputs are ANDed; if all three J-inputs are high, the Q output is high after the clock pulse. The K-inputs activate the Q output similarly. If the J and K inputs are both driven to clear their respective outputs (all low), there Is no change-of-state after the clock pulse. But, if the J and K inputs are both set to activate their respective outputs (all high), there is a change-of-state in response to the clock pulse.

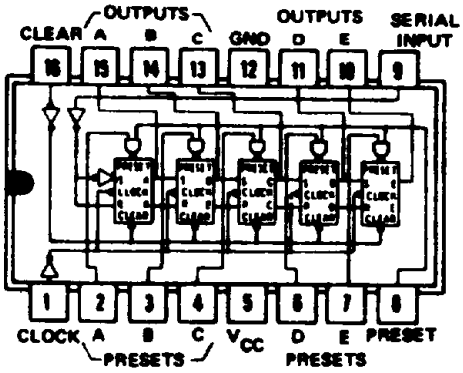
l. SN7486 Quadruple Two-Input Exclusive-OR Gate. (See figure 4-9.) The SN7486 Integrated circuit contains four Identical positive logic two-input exclusive-OR gates. The output of each such gate is at logic high only when one of its inputs is at logic high. If both inputs are high or low, the output is low. Connections are shown in figure 4-9.

m. SN7490 Decade Counter. (See figure 4-9.) The SN7490 integrated circuit contains logic which can act as separate divide-by-two and divide-by-five counters. Both counters are provided with a pair of dual reset inputs. These provisions allow external connections or (lack of them) which allow this integrated circuit to function as: separate divide-by-two and divide-by-five counters, as a divide-by-ten binary counter, and as a binary coded decimal decade counter. Connections are shown in figure 4-9. First stage output, A, is input divided-by-two. Second stage input is, DB; fourth state output, D, is BD divided-by-five. If the A output is connected to the BD Input, then the A through D outputs are a BCD count of serial data entered at Input A. If the D output Is connected to the A input, then output A is input BD data divided-by-ten. If logic high Is applied to both R_o. inputs and at least one R_9 input is at logic zero, outputs A through D are logic low. If logic high is applied to both R_9 inputs, outputs A through D represent a nine's complement.

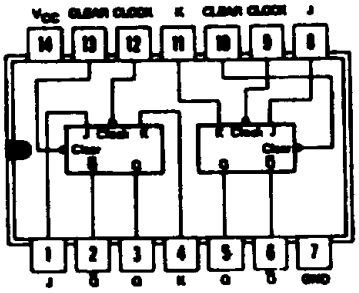
n. SN7494 4-Bit Shift Register. (See figure 4-10.) The SN7494 integrated circuit provides serial output of either of two 4-bit parallel inputs or a 4-bit serial input, under clock control. Several of these registers can be cascaded to make a register more than 4 bits long. As shown in figure 4-10, a clear input is provided, application of logic low to this input puts zeros in all bit positions. Either of the two parallel 4-bit inputs is loaded by application of logic high to the respective unlettered preset (PRI, PR2) input. Subsequently, this data is transferred out one bit at a time each time clock signal goes positive. Data at the serial input enters the first register stage each time clock signal goes positive.



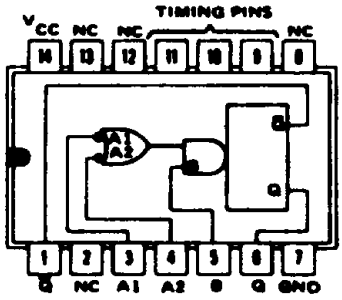
a. (SN7494)



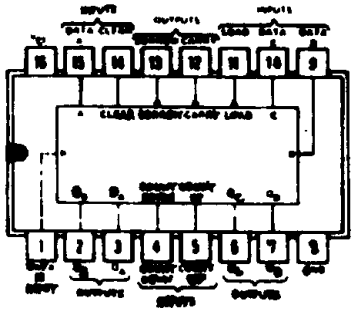
b. (SN7496)



c. (SN74107)



d. (SN74121)



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e. (SN74193)

Figure 4-10. Integrated Circuit Connections

o. SN7496 5-Bit Shift Register. (See figure 4-10.) The SN7496 integrated circuit provides serial input/output or parallel input/output of five data bits under clock control. Several of these registers can be cascaded to make a register more than 5 bits long. As shown In figure 4-10, a clear input is provided. Application of logic low to this input puts zeros in all positions. Parallel data is loaded into the register through the preset A through D inputs when preset is at logic high (independent of clock). This data is transferred to the register outputs when clock signal goes positive. Data at the serial input is loaded into the first register stage each time clock goes positive. Each time the clock goes positive, data is shifted one stage to the right. Consequently, output E provides serial data output.

p. SN74107 Dual J-K Master-Slave Flip-Flop. Connections are shown in figure 4-10. For each flip-flop, two asynchronous inputs (preset and clear), and two synchronous inputs (J and K) are provided. Response to preset and clear inputs is Independent of clock signal. When the preset input Is at logic low, it sets the Q output to logic high. When the clear input is at logic low, it sets the Q output to logic high. When the clear input Is at logic low, it sets the Q output to logic high. The preset and clear inputs have priority over the J-K inputs, which are transferred to the output after the clock pulse voltage reaches a particular level, if preset and clear are both high. If the J input is high, the Q output is high after the clock pulse. Similarly, high K input activates Q output after clock pulse. If J and K inputs are both low upon clock pulse, there is no change of state. But if J and K inputs are both high upon clock pulse, flip-flop output changes state.

q. SN74121 Monostable Multivibrator. (See figure 4-10.) The SN74121 integrated circuit contains a pulse-forming monostable multivibrator (single-shot). Connections are shown in figure 4-10. Pulse duration and duty cycle is determined by an external resistor/capacitor network. Positive pulse (Q) and inverted (notch, Q) outputs are provided. The single-shot produces an output when triggered by an input signal. Inputs for positive-going and negative-going trigger signals are provided. A positive-going signal, B, triggers the single-shot when it reaches a certain voltage, but one negative-going input, Al or A2, must be biased to logic low. A negative-going signal at either Al or A2 (or both) triggers the single-shot upon reaching logic low when B is at logic high. Output pulse duration is independent of input pulse duration and amplitude. With no timing network, output pulse is typically 30 nanoseconds. Durations from 40 nanoseconds to 40 seconds are available with network values given by the expression:

$$t = C \bullet R \bullet \log_e 2.$$

r. SN74193 Synchronous 4-Bit Up/Down Counter. (See figure 4-10.) The SN74193 integrated circuit can function as a 4-bit upcounter or downcounter. The counter can be preset with a 4-bit binary count, on command. As shown in figure 4-10, a clear input is provided. If logic high is applied to the clear Input, all counter outputs are set to logic low. Borrow and carry outputs are provided to allow cascading of stages to accomplish larger counts. The borrow and carry outputs occur for the duration of countdown and countup inputs when the counter is empty or full, respectively. The countup and countdown Inputs increment or decrement counter contents one bit at a time, respectively. Counter contents are preset from data input signals when a logic low is applied to the load Input.

s. DM8551 Bus OR'able Quad-D Flip-Flop. (See figure 4-11.) The DM8551 Integrated circuit contains four identical d-type flip-flops and control logic. As shown in figure 4-11, all four flip-flops operate from the same clock and clear signal inputs. In addition, NORed pairs of input disable and output disable control Inputs are provided: disabled outputs exhibit

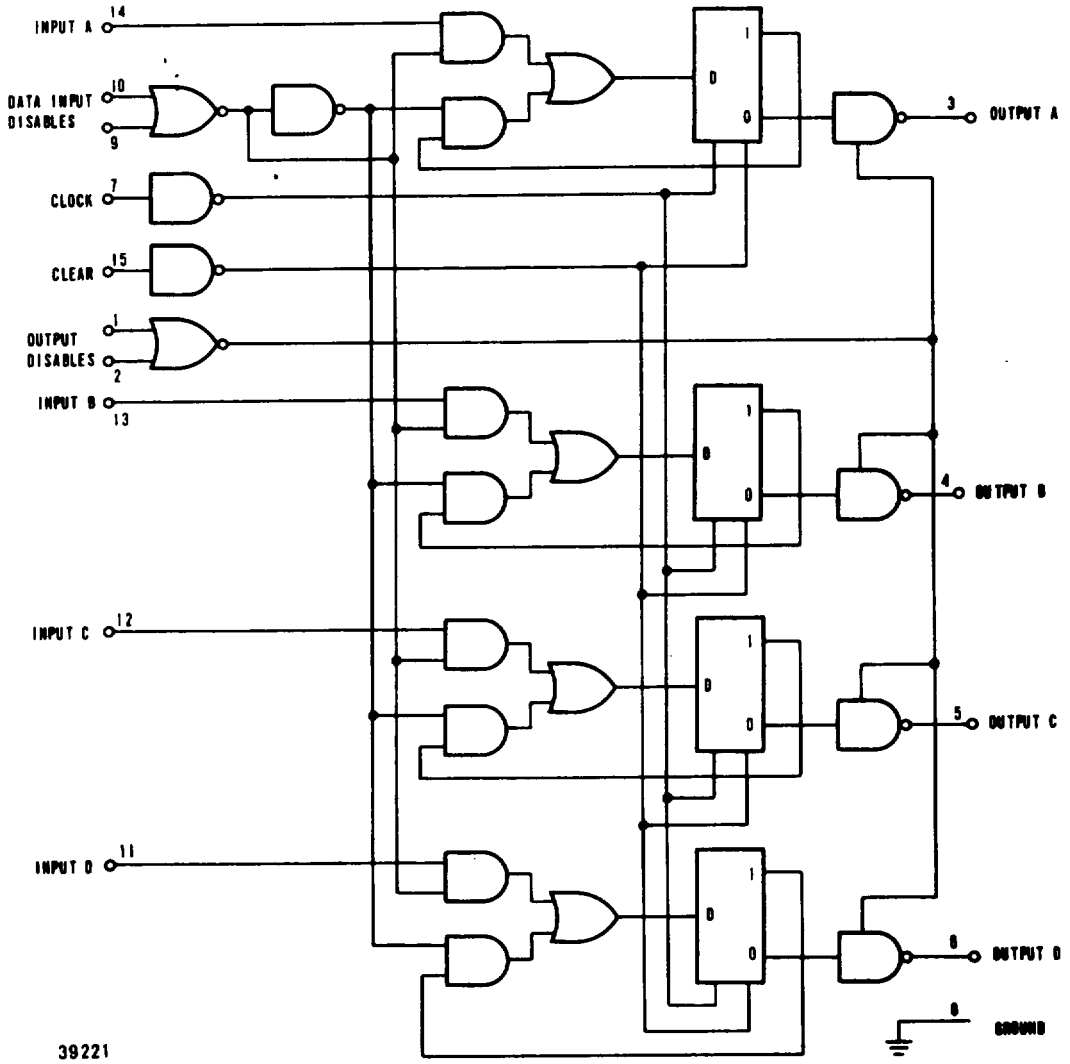


Figure 4-11. Integrated Circuit Connections (DM8551)

high impedance; enabled outputs are logic high or logic low (depending on stored data) and low impedance. The high-impedance when-disabled third logic state allows operation of many of these integrated circuits in parallel where output is enabled from only one at time. The NOR gate in the output-disable control line aids in decoding of external selection commands for such use. Logic high signal at a disable input inhibits response. Input signals are normally routed directly through control logic to the flip-flop inputs. Flip-flop inputs are accepted when clock signal goes positive. All outputs are made logic O when a logic high is applied to the clear input. If a data input disable signal is at logic high when clock signal

goes positive, flip-flop Q output is routed back to the respective flip-flop input; input data is inhibited from entering the flip-flop. Consequently, the flip-flops cannot change state when a data input disable signal is high.

t. MC4024P Voltage-Controlled Multivibrator. (See figure 4-12.) The MC4024P integrated circuit contains two identical and independent multivibrators. The frequency of each square wave output is controlled by the voltage of a control signal. Frequency is variable over a 3.5-to-1 range; the range is determined by the size of an external capacitor. The value of the capacitor and upper and lower frequency limits are given by the equations:

$$C_{(f)} = \frac{500}{\text{Freq.}_{(\text{max, Hz})}}$$

and

$$C_{(f)} = \frac{100}{\text{Freq.}_{(\text{min, Hz})}}.$$

Maximum operating frequency is 25 MHz, and control voltage can be +1 volt dc to +5 volts dc. Each multivibrator Is provided with a buffer to provide standard logic level outputs. Both buffers are operated from the same power input terminal. Each multivibrator operates from a separate power Input terminal. Connections are shown In figure 4-12.

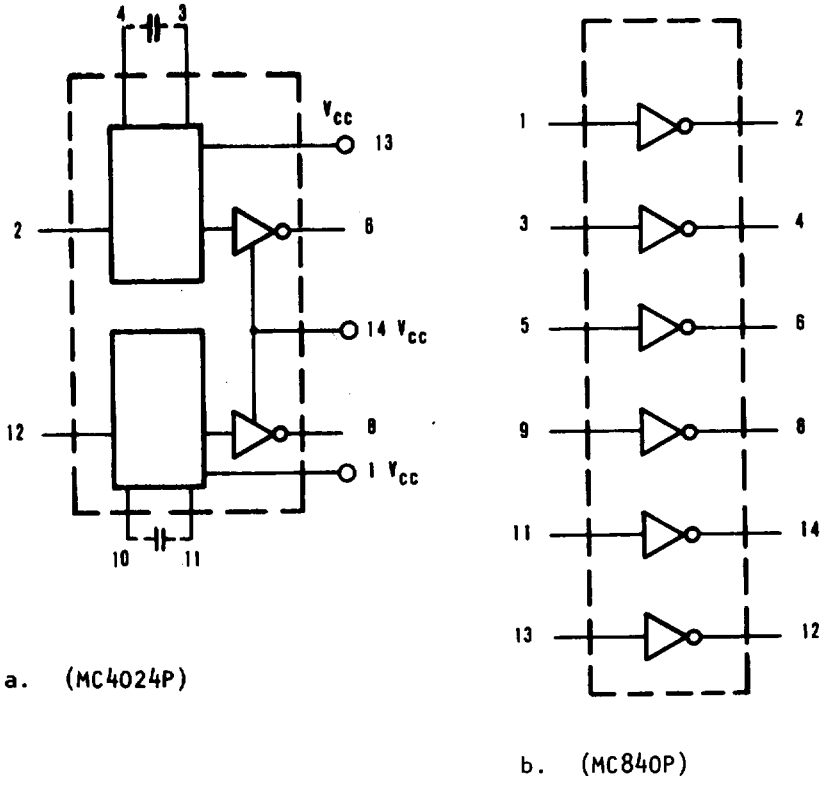


Figure 4-12. Integrated Circuit Connections

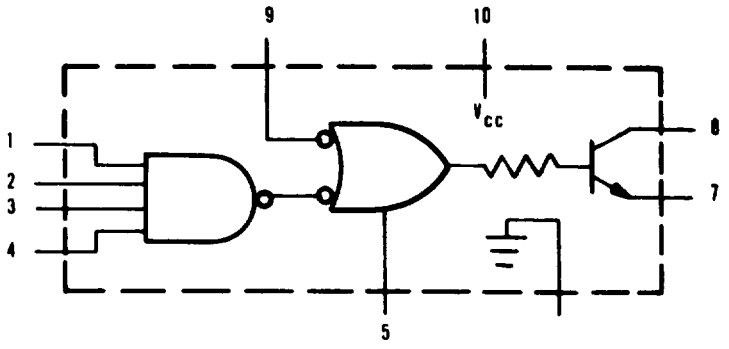
u. MC840P Hex Inverter. (See figure 4-12.) The MC840P Integrated circuit contains six identical signal inverters with no input diodes. The lack of Input diodes makes this integrated circuit unsuitable for use with long signal lines. The output logic level for each inverter is opposite its respective input logic level. Connections are shown in figure 4-12.

v. NH0017CN High-Voltage High-Current Driver. (See figure 4-13.) The NH0017CN integrated circuit contains a positive logic four-input NAND gate, a positive logic NOR gate, and an NPN transistor. As shown in figure 4-13, NAND gate output is routed to one of the NOR gate inputs. The NOR gate output Is externally available and is also routed through an isolation resistor to the transistor base. The NOR gate is provided with an expansion input through which it acts as a positive logic OR gate. The NOR gate output is at logic high if expander Input is at logic high, NOR input is at logic low, and/or NAND gate output Is at logic low. The NAND gate output is at logic high unless all of its inputs are at logic high. High output from the NOR gate enables conduction in the transistor If its emitter is biased to ground or a lower voltage. Both emitter and collector are available for external connection as required. The transistor is capable of switching a 50-volt source, and can carry 500 milliamperes continuously (2 amperes in a pulse).

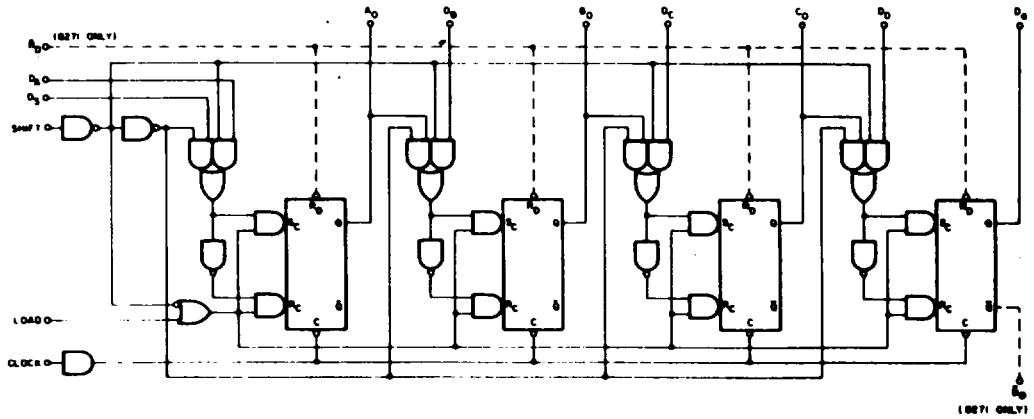
w. 3300-44028-1 Diode Matrix. (See figure 4-14.) The diode matrix consists of arrays of passivated silicon diodes. The cathode of each diode in a matrix row is connected directly to a common connection. The anode side of each diode in a matrix row is connected to a common connection through a fusible link. By selectively opening fuses, diodes are effectively removed from the circuit to form a desired matrix pattern. The basic diode matrix is either a Radiation Diode Matrix RMI-0186-5 or a Texas Instrument Diode Matrix DM-108. The fusible links are removed by F & M Systems Co. engineers to provide the desired matrix pattern. Three diode matrices are prepared in this manner to provide the three F & M Systems Co. Diode Matrices 3300-44028-1, 3300-44029-1, and 3300-44030-1. These diode matrices are identified as U1, U2, and U3, respectively, in the bsu/biu A1 circuit card (3300-44056) and in the special project bsu/biu A2 circuit card (3300-44118-1).

x. N8271B 4-Bit Shift Register. (See figure 4-13.) The N8271B Integrated circuit provides serial or parallel output of a 4-bit serial or parallel input. Connections are shown in figure 4-13. The RD Input is for clearing register contents; if logic low is applied to the WD input, the register outputs are logic low. Parallel inputs DA through DD are stored on negative-going clock signal when logic high is applied to the load Input. Register outputs are always present, but shift through the register 1 bit at a time in response to clock signal when logic high is applied to the shift input. As data shifts through the register, serial present at the DS input is loaded into the first register stage. Serial data is provided at the Do and Do outputs.

y. U7D961459X Dual Differential Line Driver. (See figure 4-14.) The U7B961459X integrated circuit contains two Identical circuits designed to drive long transmission lines in response to single-ended logic level inputs. As shown in figure 4-14, each identical circuit is provided with a three-input AND/AND gate. When all three inputs are at logic high, the gate provides a complementary pair of signals which drive amplifiers. Each amplifier has two outputs (one for pull-up and the other for pull-down) to allow wired-OR function with single-ended or differential operation. Differential operation is accomplished by connecting the two outputs of each amplifier together.



a. (NH0017CN)



b. (N8271B)

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Figure 4-13. Integrated Circuit Connections

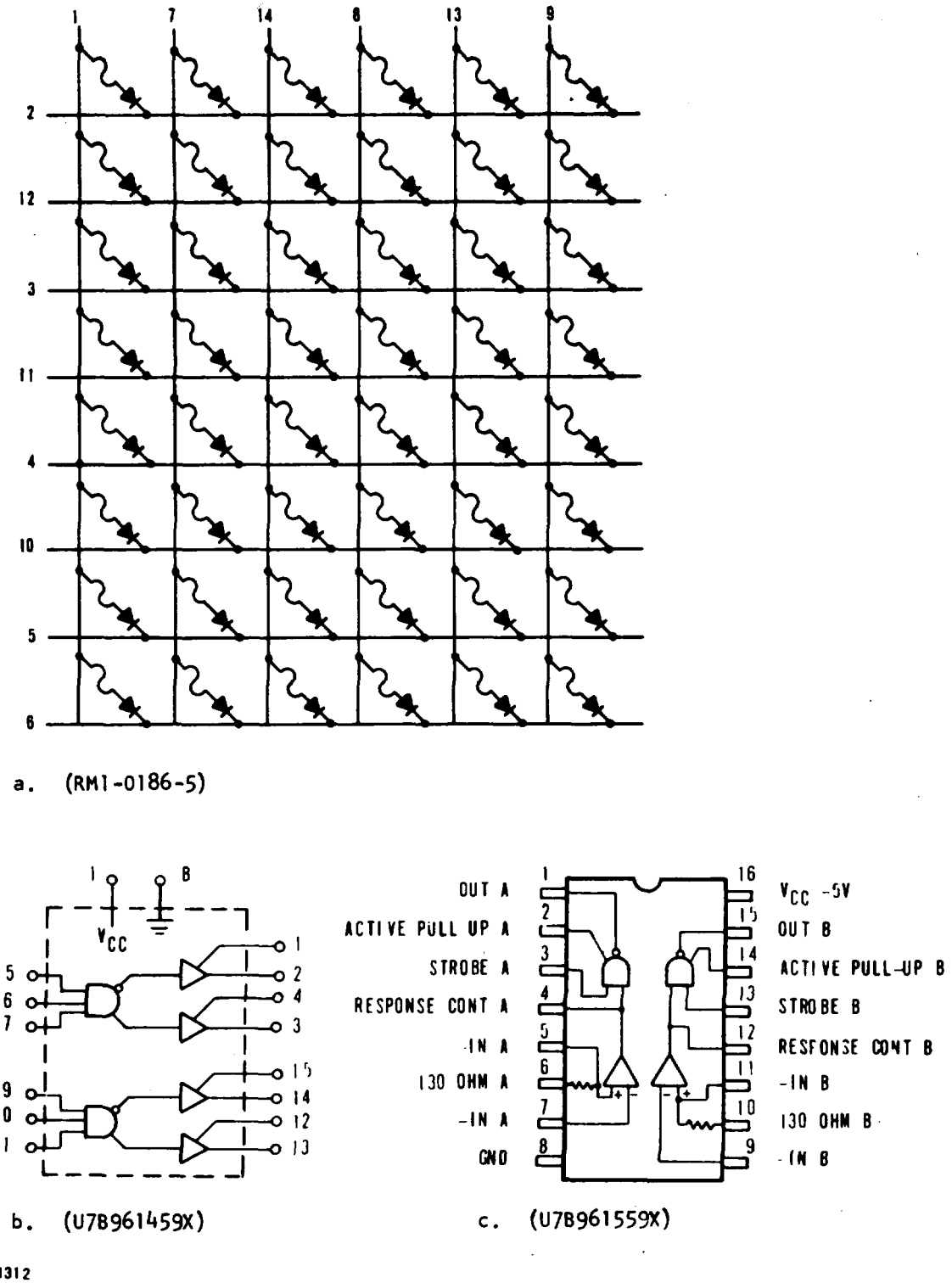

Figure 4-14. Integrated Circuit Connections

z. U7B961559X Dual Differential Line Receiver. (See figure 4-14.) The U7B961559X integrated circuit contains two Identical circuits designed to accept differential line signal and provide corresponding single-ended logic level signals. As shown in figure 4-14, line input to each receiver is to a differential amplifier. A line terminating resistor is available for external connection. Differential amplifier output is brought to a terminal and to an AND/NAND gate. Differential amplifier output, called response control, can be slowed down by connection of an external capacitor. A second input to the AND/NAND gate provides for strobe control of received data. When both of its inputs are high, the AND/NAND gate provides a complementary pair of outputs. One output is the open collector type. The second output, called active pull-up, can be connected to the first output to provide discrete two-level logic output.

SECTION V

MAINTENANCE AND REPAIR

5-1. Scope.

This section describes maintenance duties assigned to the operator and the unit repairman. Maintenance duties assigned to the operator consist primarily of preventive maintenance with limited troubleshooting and repair. Maintenance duties assigned to the unit repairman consist of preventive and corrective maintenance on equipments within the intercept group and checkout and repair of these equipments.

5-2. Non-Maintenance Items.

Non-maintenance items are defined as those items that are either repairable at the factory where they originated or are throw-away items. In either case, they are considered beyond the local repair capability. Non-maintenance items are identified on equipment illustrations by leader lines and appropriate note references.

5-3. Preventive Maintenance. (See table 5-1.)

Preventive maintenance Is the systematic care, servicing, and inspecting of equipment to prevent the occurrence of trouble, reduce downtime, and assure that the equipment is serviceable. Table 5-1 lists the maintenance routine and recommended periods when maintenance should be performed.

Table 5-1. Maintenance Schedule

Period	Procedure
Daily	1. Perform BAND/AZIMUTH lamp test by pressing LAMP TEST. Replace the BAND and AZIMUTH lamps which do not light.
	2. Momentarily press NO-BEAM switch. Observe that the NO-BEAM lamp lights, the azimuth and band remain the same, and signal is lost at the receiver.
Monthly	1. Momentarily press FAULT switch. Observe that the FAULT Monthly lamp lights and that the bsu/biu address and location is printed on the somc tty machine.
	2. Use multimeter to measure 5 ± 0.5 volts dc at output pins of each power supply in the bsu/biu's, substations, and special project bsu/biu's.
	3. Use a clean cloth to remove dust, dirt, moisture, and grease from the exterior surface of the unit.
	4. Use a vacuum cleaner to vacuum the interior surface of the unit.

Table 5-1. Maintenance Schedule (Continued)

Period	Procedure
	5. Check to see that all cable connectors are firmly seated. 6. Check that the mechanical operation of each switch is smooth and free of external binding.

5-4. Maintenance Test Equipment (See table 5-2.)

Test equipment required to perform corrective maintenance procedures is listed in table 5-2.

Table 5-2. Test Equipment Required

Nomenclature	Common Name	Use
Test Set Beam Selection-Identification Unit TS-3283-FLR-9(V)	Bsu Test Set	Provides necessary signals for troubleshooting the bsu/biu and substation.
Oscilloscope TEK Model 140A	Oscilloscope	Used to measure signals while troubleshooting all units in the intercept group.
Simpson 260-5 Multimeter	Multimeter	Used to measure voltage while troubleshooting power supplies used in the intercept group.
Digital Test Set AN/FLM-47	Digital Test Station	Provides test facility for repair of bsu/biu and substation
Cable, Multiconductor 3300-68033-2 and 3300-68033-1	Test Cables	Provides signal path between test set, and substation, or bsu/biu.
None	Dummy Plug (t to w)	Replaces Multiconductor cable 3300-40008-2 when bsu/biu test set calibrator is not In use.

Table 5-2. Test Equipment Required (Continued)

Nomenclature	Common Name	Use
Cable, Multiconductor 3300-40008-2	Test set calibrator cable.	Used to connect the bsu test set to the bsu test set calibrator.
Calibrator, Beam Selection-Identification Unit TS-3284/ FLR-9(V)	Test set calibrator	Used to drive bsu test set at a 1-cycle rate.

5-5. Special Maintenance Tools.

No tools other than normal shop tools are required to perform maintenance, repair, and alignment procedures.

5-6. Corrective Maintenance.

Corrective maintenance for the unit repairman consists of isolating a fault to a bsu/biu, a substation,or the.position scanner in the intercept group. Once this faulty equipment is identified, it is replaced by a known good unit. Corrective maintenance is continued by isolating a faulty component (replaceable item) in the equipment. Repair of the equipment is then accomplished by removing and replacing the faulty component. A check of the equipment operation is then effected by performing the minimum performance standard procedures.

5-7. Logical Troubleshooting Procedures.

a. General. As a first step in isolating a fault in the intercept group, sectionalize the fault. In this step, the fault is traced to an equipment (bsu/biu, substation, or position scanner). The second step is to localize the fault. In this step the equipment is checked to identify a faulty subchassis, module, circuit card, or component part in the equipment.

b. Sectionalization. Determine which unit is likely to be faulty by noting the nature of the fault. All bsu/biu's operate with the position scanner. So, it all bsu/biu have common symptoms, the most likely circuit to suspect is the position scanner. Groups of eight bsu/biu operate with a particular (common) substation. So, if eight bsu/biu have the same fault, the most suspicious item would be the substation. If only one position has a fault, it may be due to failure in that bsu/biu, in its substation, or in the cable between them. If a unit in the chain cannot be identified as being faulty, it may be necessary to substitute equipment. First, use a bsu/biu with the common substation. If the fault is corrected, the original bsu/biu is probably faulty. If the fault remains, the substation or the position scanner must be suspected as the faulty unit. If so, use a bsu/biu associated with another substation. If this bsu/biu receives beam request data, the original substation is probably faulty If this bsu/biu receives no beam request data, the position scanner is probably faulty.

c. Localization. Localization procedures should be performed after the faulty equipment has been identified. The methods that aid in localizing a fault to a subchassis, module, circuit card, or component part include the following.

1. Visual Inspection. Faults such as burned out resistors, overheated transistors, and arcing or shorted transformers can often be located by sight, smell, and hearing. Carefully observe front panel indications, as inoperative lamps and switches may be used as an aid in localizing a fault.

2. Operational Tests. Operational tests provide step-by-step procedures used to localize a fault. Operating configuration of both the test equipment and equipment under test is provided by presetting front panel controls. Test parameters are provided by front panel indications, waveform, and voltage parameters. Perform all steps in the operational tests in the sequence listed. Be careful to set all switches in the position listed. Operational test for the intercept group is contained in paragraph 5-8. Operational tests for the bsu/biu, special project bsu/biu, and the substation are contained in paragraphs 5-9, 5-11, and 5-13, respectively. Troubleshooting procedures for the position scanner are contained in paragraph 5-15. The common 5-volt dc power supply troubleshooting data is contained in paragraph 5-16.

3. Troubleshooting. Visual inspection and operational tests provide a systematic method of localizing a fault. Additional information leading to localizing a fault is contained in the troubleshooting chart.

4. Performance Standards. Performance standards provide indications, readings, and tests to indicate to the unit repairman that the equipment provides minimum acceptable results. Minimum performance standards for the intercept group equipment are contained in paragraph 5-19.

5-8. Intercept Group Operational Tests.

The intercept group operational test provides procedural steps to localize a faulty unit in the intercept group. Carefully perform the steps in sequence, ensuring that switches are set properly before proceeding. When test results are not as required, refer to the applicable operational tests as indicated in the procedural steps.

NOTE

The following procedural steps rely on the system control group for control, requests, and responses. These controls, requests, and responses route eight signals through the position scanner and the substation for use by the bsu/biu. In passing through these units differential line drivers and single-ended inverters amplify the eight signals. These amplifiers, if open, could make it appear as if a bsu/biu or substation were faulty when the fault could be an amplifier in the substation or in the position scanner.

a. System lockup can be evidenced by a priority 13 lockup at the computer. The priority 13 lockup Is caused by the computer attempting to service a request by the position scanner and failing in the attempt. This can be caused by a continuous request being inputted to the position scanner. Another system lockup can be evidenced by all bsu/biu being unable to request a beam because the CLOCK pulse is attenuated at some common point. A data line attenuation at some

common point might provide the same symptoms. In either of these cases remove all Inputs to the position scanner by disconnecting input cables. If necessary, reload the program. After removing all inputs, replace them one at a time. As each is replaced, determine that the bsu/biu's associated with the input are operational. Continue this procedure until the bsu/biu or substation causing the symptom is noted.

b. At the substation associated with the suspected bsu/biu, ensure that the POWER switch is set to ON.

c. At the suspected bsu/biu, perform the following steps.

1. Remove the switch cover and ensure that the proper address is set in the ADDRESS SELECTION switches.

2. Ensure that the POWER switch is set to ON.

3. Press and hold DISPLAY LAMP TEST switch while observing all 8's in the BAND and AZIMUTH indicators.

4. Momentarily press NO BEAM and observe that the indicator lights.

5. Momentarily press FAULT and observe that the indicator lights, fault message is output on the tty, and NO BEAM lamp is extinguished.

NOTE

Ensure that all indicators are operating properly before proceeding.

6. Momentarily press the following:
   (a) RCVR 1.
   (b) BEAM SELECT 1.

7. Observe BAND and AZIMUTH for requested beam data.

8. If requested beam data Is correct proceed to step 9% If requested beam data is not correct proceed to step 25.

9. Momentarily press the following: (a) RCVR 2 (b) BEAM SELECT 2.

10. Observe BAND and AZIMUTH for requested beam data.

11. If requested beam data is correct proceed to step 12; if requested beam data is not correct, the bsu/biu is faulty.

12. Momentarily press RCVR 1.

13. Observe BAND and AZIMUTH for the beam data requested In steps 6 and 7.

14. If requested beam data is correct, proceed to step 15; if requested beam data is not correct, the bsu/biu is faulty.

15. Momentarily press RCVR 2.

16. Observe BAND and AZIMUTH for beam data requested in step 9.

17. If data is correct proceed to step 18. If data is incorrect the bsu/biu is faulty.

18. Press FAULT.

19. Observe the FAULT message on the somc tty machine (Fault at OPER XXX, RCVR Y where X is the operator position and Y is receiver 1 or 2).

20. If the FAULT message Is correct, the position scanner is operational, the substation circuitry associated with this bsu/biu is operational, and the bsu/biu is operational. If the FAULT message is not present, the bsu/biu is faulty.

21. Repeat steps 6.and 7. using another bsu/biu connected to the same substation.

22. If the requested beam data is incorrect, this bsu/biu is faulty.

23. Repeat steps 6.and 7. using another bsu/biu and another substation.

24. If the requested beam data is correct, this circuit is operational. If the requested beam data is not correct, the substation or bsu/biu is faulty.

25. Repeat step 6. using RCVR 2.

26. If requested beam data is correct, the bsu/biu is faulty; if requested beam data is incorrect, proceed to step 27.

27. Repeat step 6. using a different bsu/biu associated with the same substation.

28. If requested beam data is correct, the original bsu/biu is faulty. If requested beam data is incorrect proceed to step 29.

29. Repeat step 6. using a bsu/biu associated with another substation.

30. If the requested beam data is correct the substation is faulty. If the requested beam data is incorrect the positive scanner is faulty.

31. Replace the ADDRESS SELECTION switch cover.

d. If the suspected unit is a special project bsu/biu, perform the following steps.

1. Ensure that the proper address is set in the ADDRESS SELECTION switches.
2. Ensure that the POWER switch is set to ON.
3. Press and hold DISPLAY LAMP TEST switch while observing all 8's in the BAND and AZIMUTH indicators.

NOTE

Ensure that the BAND and AZIMUTH Indicators are operating properly before proceeding.

4. Momentarily press BEAM CLEAR. Observe that MODE SELECT and FAULT indicators are extinguished.
5. Momentarily press FAULT. Observe that the FAULT indicator lights.
6. Momentarily press BEAM CLEAR and observe that the FAULT lamp is extinguished.
7. Momentarily press MON BEAM and observe that the indicator lights.
8. Momentarily press BEAM CLEAR and observe that the lamp is extinguished.
9. Repeat steps 7.and 8.using SECTOR BEAM and OMNI BEAM, respectively.

NOTE

Ensure that all indicators are operating properly before proceeding.

10. Momentarily press the following.
    (a) MON BEAM
    (b) BAND SELECT A
    (c) BEAM SELECT DEGREES to select known signal
    (d) BEAM SET

11. Observe BAND and AZIMUTH for requested beam data of nearest available beam.

12. If requested beam data is correct, proceed to step 13.; If requested beam data Is not correct, proceed to step 16.

13. Press BEAM CLEAR.

14. Observe desired signal in associated receiver.

15. If desired signal Is heard, the special project bsu/biu and the associated circuitry in the substation and position scanner are operational. If desired signal is not heard, the special project bsu/biu Is probably faulty.

16. Repeat steps 10. and 11. using another bsu/biu or special project bsu/biu connected to the same substation.

17. If the beam data Is correct, the suspected special project bsu/biu is faulty. If the beam data Is not correct, proceed to step 18.

18. Select a bsu/biu associated with a different substation and perform the following: Momentarily press RCVR 1 and BEAM SELECT 1.

19. If the requested beam data is correct, the suspected substation is probably faulty. If the requested beam data is not correct, the position scanner is probably faulty.

e. To see if the computer and position scanner are honoring beam requests, use the bsu/biu in the SOM Console to test for beam selection (V8 only).

f. To check a bsu/biu before returning it to service, connect it to the bsu/ biu substation in the SOM Console (V8 only).

g. To check the position scanner for failure involving one or more substations, use the substation and bsu/biu at the SOM Console (V8 only).

h. To quickly check connections at the patch field and/or RF switch paths, use the receiver in the SOM Console to compare relative amplitudes (V8 only).

5-9. Bsu/Biu Performance Tests. (See figures 5-1, 5-2, and 7-4.)

The bsu/biu performance tests provide procedural steps to localize a faulty circuit card in the bsu/biu. Test setup is shown in figure 5-1. Carefully perform the steps in sequence. When a defective card is located, refer to Card Repair Manual, IM 32-5895-239-15, for repair procedures. Parts location is provided in figure 5-2.

a. At the digital test station, connect the bsu/biu to the bsu test set as shown in figure 5-1.

b. At the bsu/biu, perform the following.

1. Set POWER switch to ON.

2. After removing switch cover, set ADDRESS SELECT switches to 010101010.

3. Momentarily press RCVR 1 switch.

4. Use a multimeter to measure 5 $\pm$ 0.5 volts dc between A4-60 and chassis ground. If the voltage is not within tolerance, perform power supply troubleshooting outlined in paragraph 5-16. If the voltage is within tolerance, perform the next step.

5. Use oscilloscope to measure no more than 50 millivolts ripple between A4-60 and chassis ground. If the ripple is greater than 50 millivolts, perform procedures in paragraph 5-16. If the ripple is within tolerance, perform the next step.

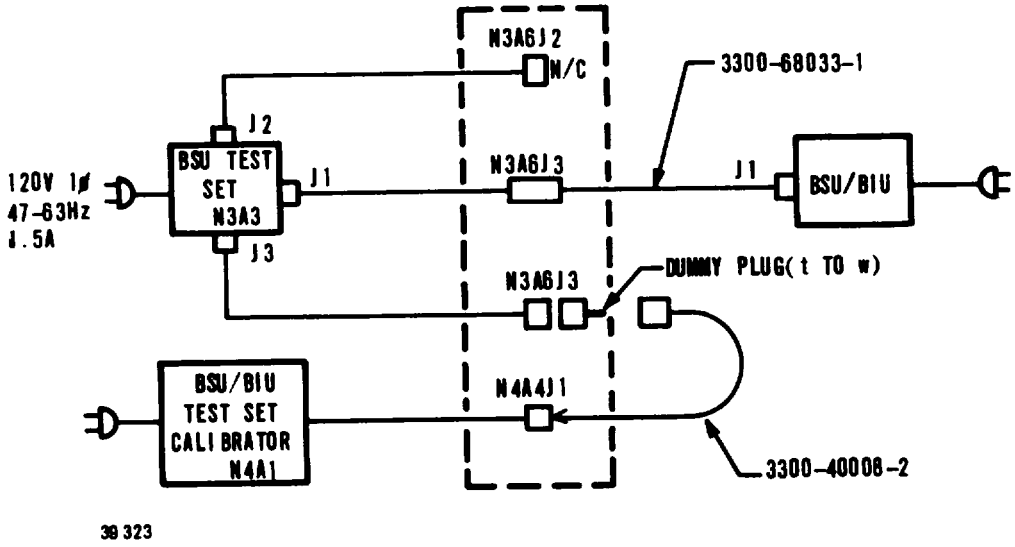

Figure 5-1. Bsu/Biu and Special Project Bsu Test Setup

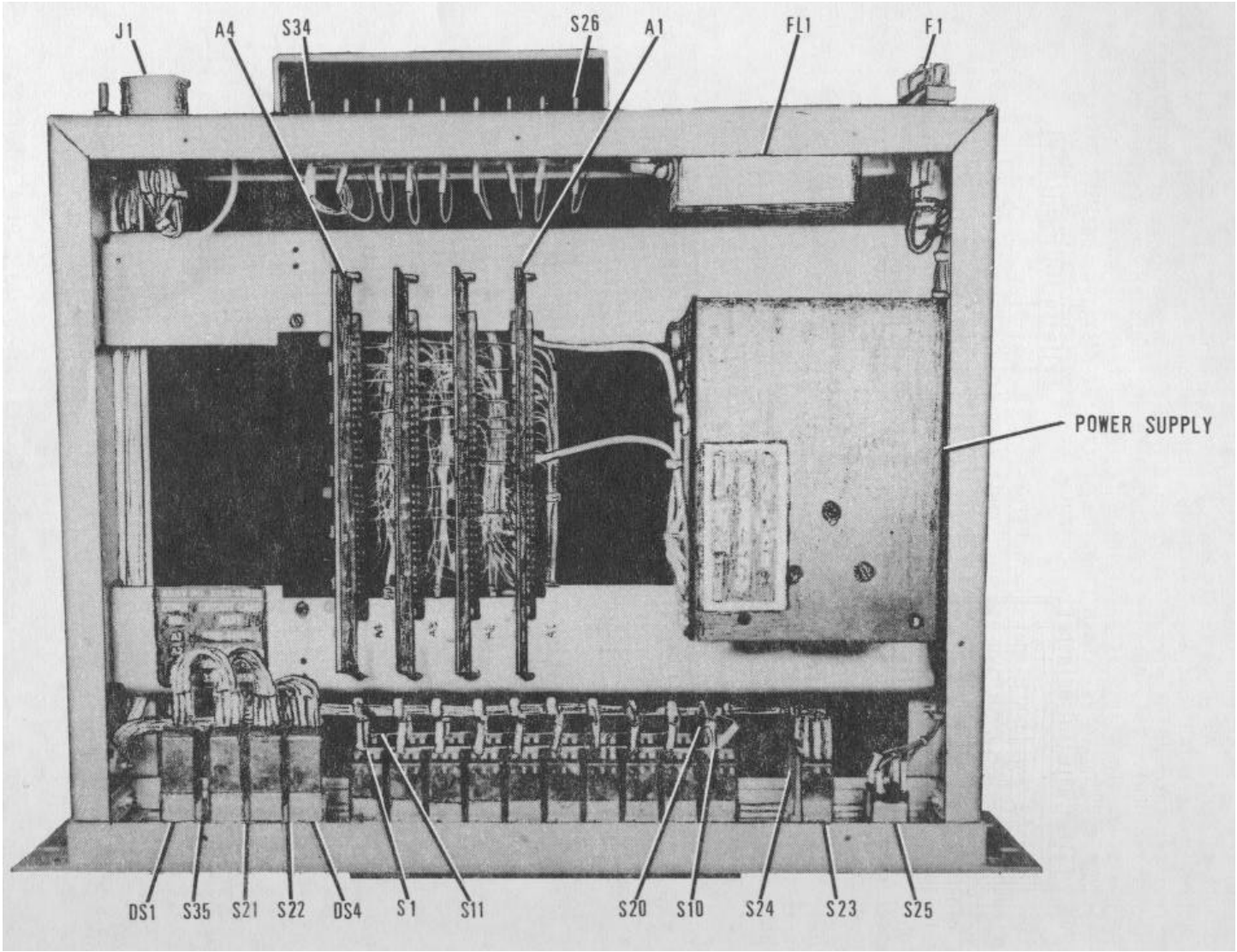

Figure 5-2. Bsu/Biu Parts Location

6. Press DISPLAY LAMP TEST switch and observe a figure 8 in the BAND AND AZIMUTH display lamp.

7. If figure 8's are displayed proceed to step c. If figure 8's are not displayed in each indicator, proceed to step 8.

8. If lamps fail to light, replace appropriate bulbs. If lamps continue to remain off, replace appropriate fiber optic circuit clip. Refer to paragraph 5-17.h. for removal procedures.

c. At the bsu test set, perform the following.

1. Set POWER switch to ON.
2. Set ADDRESS SELECT switches to 010101010.
3. Set BSU-SUB/STA switch to BSU.
4. Momentarily press ADDRESS ENTER switch.
5. Set RCVR l/RCVR 2 switch to RCVR 1.
6. Set BAND switch to A.
7. Set AZIMUTH switches to 000.
8. Set FAULT-OFF switch to OFF.
9. Momentarily press REPLY switch.
10. Momentarily press INTRG and RUN switch.

d. Signal trace the bsu/biu as follows.

1. Using the oscilloscope on internal sync, measure the CLOCK square wave at A4-40 (ID6C).
2. If CLOCK is present proceed to step 3. If CLOCK is not present, check the test setup and/or bsu test set.
3. Connect the sync input of the oscilloscope to A4-40 (ID6C) and adjust the oscilloscope for external sync. (Internal sync may be used if desired.) 4. Measure CLOCK-P at A4-39 (ID6C). If not present, replace card A4.
5. Momentarily press test set REPLY and RUN switches. Measure SERIN address data pulses at A4-37 (ID6A). If the address pattern is present, proceed to step 16.

If not present, check test setup and/or bsu test set.

6. Measure SERIN-P at A4-38 (ID6A). If not present, replace card A4.
7. Momentarily press INTRG and RUN switches on test set. Measure address pattern 110101010 at output of storage register consisting of AIU6 through AIU8 (ID4A and ID6B). If not present, replace card Al.
8. Measure CLEAR pulse at A3-19 (2E7A). If pulse is present, proceed to next step. If pulse is not present, check test setup and/or bsu test set.
9. Measure CLEAR B-N pulse at A3-22 (2E7B). If pulse is not present, proceed to next step.
10. Measure ADDRESS pulse at A4-20 (1G3A). If ADDRESS is present, proceed to step 11. If ADDRESS is not present, check the test setup and/or the bsu test set.
11. Measure ADDRESS-P at A4-53 (1G3A). If not present, replace card A4.
12. Measure ADDRCMPR-P at A4-51 (1G3C). If present, proceed to step 16. If not present, proceed to step 13.
13. Measure ADB-P at Al-32. (1G4D). If present, replace card A4. If not present, proceed to step 14.
14. Check setting of ADDRESS SELECT switches on bsu/biu and bsu test set.
15. Measure a positive level at output of address compare exclusive or circuit at area 1H4A through IF4D. Replace appropriate card A1 or A4.

NOTE

The signal appears in steps 16, 17, 19, and 20 once each time a BEAM SELECT switch is pressed while in INTRG RUN mode of test set. Therefore, a scope trace flash appears on the oscilloscope each time the BEAM SELECT switch is pressed.

16. Measure REQUEST-N output pulse at A2-42 (2FSA). If REQUEST-N is present proceed to step 23. If not present, proceed to next step.

17. Measure REQUEST-P at A3-59 (2D48). If present, replace card A2. If not present, proceed to next step.

18. Measure ADDR-P at A4-12 (2D7A). If the signal is not present, proceed to step 22. If the signal Is present, proceed to next step.

19. Measure RQST-N at A3-8 (2D5B). If pulse is not present, proceed to next step. If pulse is present, replace card A3.

20. Measure LOAD-P at A3-7 (205B). If pulse is not present, replace card A4.

If pulse is present, proceed to next step.

21. Measure DELAY-P at A4-4 (2C7B). If pulse is present, replace card A3.

If pulse is not present, replace card A4.

22. Measure PWRUPCLR-N level at A4-13 (2D7A). If level is low (O volt), replace card A3. If level is high, return to step 16 and recheck steps.

23. Change ADDRESS SELECT switches on bsu/biu and bsu test set to 101010101.

Momentarily press INTRG and RUN switch on bsu test set.

24. Measure REQUEST-N at A2-42 (2FSA) when pressing BEAM SELECT switch. (See note following step 15.) If signal is present, proceed to next step. If signal is not present, repeat steps 6,: 7, 13, 14, and 15.

25. At the bsu test set, momentarily press DATA ENTER, REPLY and RUN switches.

If BAND A and AZIMUTH 000 appears on the bsu/biu, proceed to next step. If not, proceed to step 28.

26. At bsu test set change BAND to B and AZIMUTH to 123. If BAND B and AZIMUTH 123 appear on bsu/biu, proceed to step 27. If not, proceed to step 28.

27. At bsu test set, change BAND C and AZIMUTH 246 appear on bsu/biu, the bsu/ biu is operational. if not, proceed to step 28.

28. Switch oscilloscope sync to internal; measure DATA pulse at A3-14 (2E3A). > If pulse is present, proceed to next step. If pulse is not present, check test setup and/or bsu test set.

29. Momentarily press INTG and RUN switches on test set. Measure PRESET-P at A3-10 (2E2A). If pulse is not present, replace card when pressing BEAM SELECT (See note following step 15) A3. If pulse is present, proceed to next step.

30. Measure SR CLEAR at A3-10 (2E6B). If pulse is not present, replace card A3. If pulse is present, proceed to next step.

31. Measure BT10 through BT14 while pressing BEAM SELECT switch. If positive levels at appropriate outputs are not observed, replace card Al. If level is observed, proceed to next step.

32. Measure NABLE 1-P at A3-2 (2H7A). RCVR 1 set, level is low, RCVR 2 set, level is high. If not replace card A3.

33. Replace dummy plug with patch cable 3300-40008-2 to connect test set to test set cabinets.

34. At test set calibrator set POWER to ON and CLOCK to AUTOMATIC.

35. Adjust scope sweep speed to approximately 1 second per centimeter.

36. Momentarily press Test Set switches REPLY and RUN and any one of the bsu/ biu BEAM SELECT switches.

37. Measure SER out at A2-46 (2E5A).

38. Repeat step 36 as required to determine signal levels.

39. Set ADDRESS SELECT switches to proper address and replace switch cover.

5-10. Bsu/Biu Troubleshooting. (See table 5-3 and figure 5-2.)

The bsu/biu troubleshooting table (table 5-3) provides symptoms normally observed while troubleshooting the bsu/biu. Accompanying the symptom are a number of causes and the probable remedy. If replacement of the indicated replaceable component does

Table 5-3. Bsu/Biu Troubleshooting

Step	Symptom	Cause	Remedy
1.	None of the BEAM SELECT switches causes a change of status	1. Preset signal not generated or inverter defective	Replace circuit card A3
		2. Register defective	Replace circuit card A1
2.	No switches, except LAMP TEST and POWER ON cause a change in status	1. Address recognition logic defective	Replace circuit cards A1 or A4
		2. Request logic defective	Replace circuit cards A2 or A3
3.	Some band or azimuth data is consistently	1. Input/output register defective	Replace circuit card A1 incorrect
		2. Display register defective	Replace circuit card A2
		3. Display defective	Replace defective display
4.	Band and azimuth data is consistently incorrect	1. Input/output register defective	Replace circuit card A1 correct
		2. Display register defective	Replace circuit card A2
5.	Band and azimuth data is not updated	1. Clock or clear signal not passed	Replace circuit cards A3 and A4
		2. Strobe signal not generated	Replace circuit card A3
		3. Display register defective	Replace circuit card A2
6.	Receiver selection not honored	1. Switch defective	Replace defective switch
		2. Selection logic defective	Replace circuit card A3
7.	Receiver select switches do not light when used	1. Bulb defective	Replace bulb
		2. Driver defective	Replace circuit card A4
8.	Fault or no beam switches do not light when used	1. Bulb defective	Replace bulb.
		2. Driver defective	Replace circuit cards A3 or A4

not repair the unit, normal signal tracing procedures as defined in paragraph 5-9. must be performed. If a defective circuit card is located, refer to Card Repair Manual IM 32-5895-239-15 for repair procedures. Parts location is provided in figure 5-2.

5-11. Special Project Bsu/Biu Performance Tests. (See figures 5-1, 5-3, and 7-5.)

The special project bsu/biu performance tests provide procedural steps to localize a faulty circuit card in the special project bsu/biu. Test setup is shown in figure 5-1. Carefully perform the steps in sequence. When a defective card is located, refer to Card Repair Manual IM 32-5895-239-15 for repair procedures. Parts location is provided in figure 5-3.

a. At the digital test station, connect the special project bsu/biu to the bsu test set as shown in figure 5-1. (Substitute bsu/biu with special project bsu/biu.)

b. At the special project bsu/biu, perform the following.

1. Set POWER switch to ON.
2. Set ADDRESS SELECT switches to 000.
3. Use a multimeter to measure 5 $\pm$ 0.5 volts dc between A4-60 and chassis ground. If the voltage is not within tolerance perform power supply troubleshooting outlined in paragraph 5-16. If the voltage is within tolerance perform the next step.
4. Use the oscilloscope to measure no more than 50 millivolts ripple between A4-60 and chassis ground. If the ripple is greater than 50 millivolts, perform procedures in paragraph 5-16. If the ripple is within tolerance, perform the next step.
5. Press DISPLAY LAMP TEST switch and observe a figure 8 in the BAND and AZIMUTH display lamp.
6. If figure 8's are displayed proceed to step C. If figure 8's are not displayed in each indicator, proceed to step 7.
7. If lamps fail to light, replace appropriate bulbs. If lamps continue to remain off, replace appropriate fiber optic circuit clip. Refer to paragraph 5-17.h. for removal procedures.

c. At the bsu test set, perform the following.

1. Set POWER switch to ON.
2. Set ADDRESS SELECT switches 111110000.
3. Set BSU-SUB/STA switch to BSU.
4. Momentarily press ADDRESS ENTER switch.
5. Set RCVR 1-RCVR 2 switch to RCVR 1.
6. Set BAND switch to A.
7. Set AZIMUTH switches to 000.
8. Set FAULT-OFF switch to OFF.
9. Momentarily press REPLY switch.
10. Momentarily press INTRG and RUN switches.

d. Signal trace the special project bsu/biu as follows.

1. Using the oscilloscope on internal sync, measure the CLOCK square wave at A15-34 (2F8A).
2. If CLOCK is present proceed to step 3. If CLOCK is not present, check the test setup and/or bsu test set.
3. Connect the sync input of the oscilloscope to A15-34 (ID6C) and adjust the oscilloscope for external sync (internal sync may be used if desired.)
4. Measure CLOCK-P at A14-10 (2F8A). If not present, replace card A14.
5. Momentarily press test set REPLY and RUN switches. Measure SERIN address data pulses at A15-35 (2H8A). If the address pattern is present, proceed to step 6. If not present, check test setup and/or bsu test set.

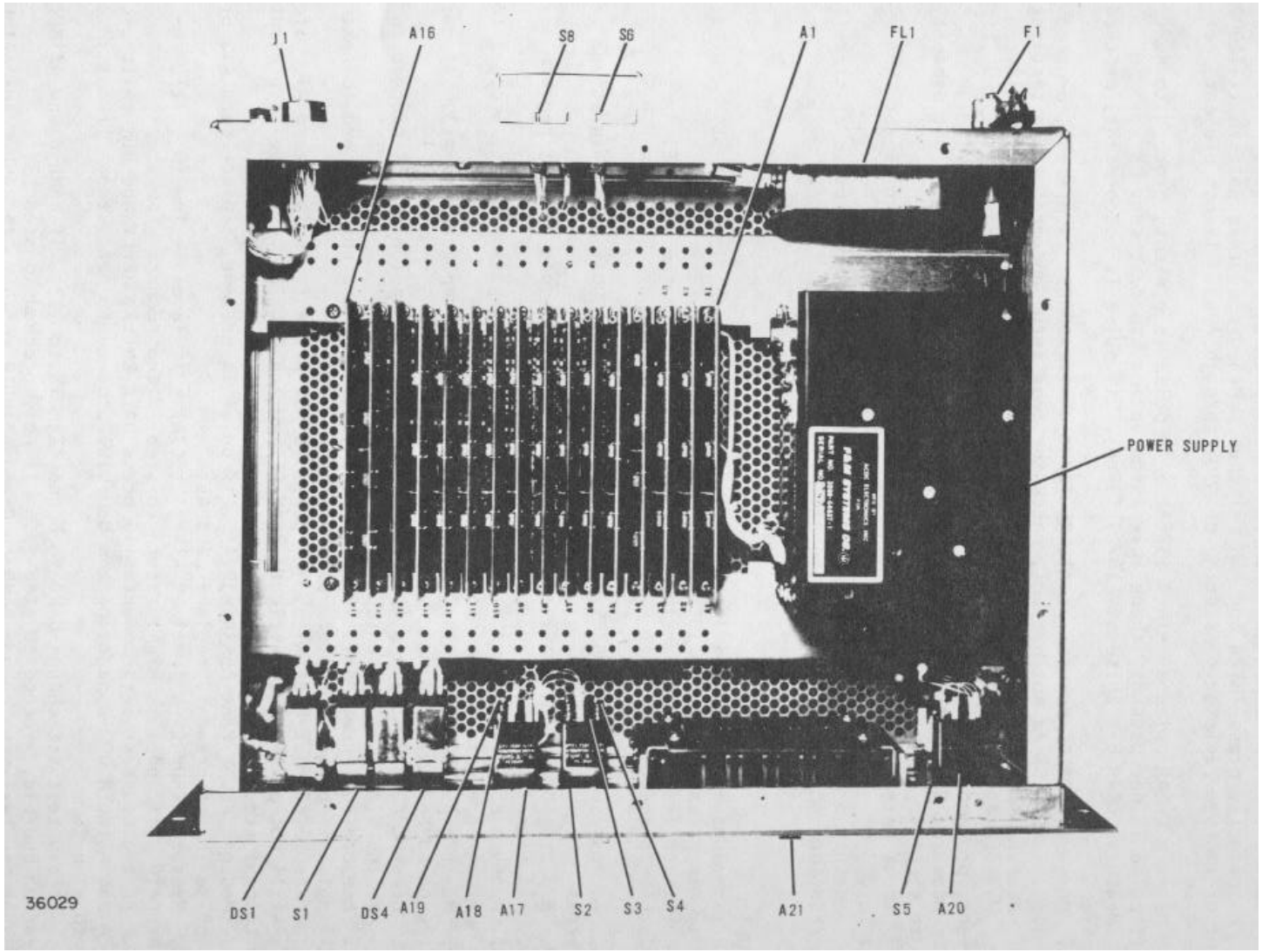

Figure 5-3. Special Projects Bsu/Biu Parts Location

6. Measure SERIN-P at A14-32 (2F8A). If not present, replace card Al4.

7. Momentarily press INTRG and RUN switches. Measure address pattern 111110000 at output of storage register consisting of A9U1 through A9U3. If not present, replace card A9.

8. Measure CLEAR pulse at A14-7 (3F8A). If pulse is present, proceed to next step. If pulse is not present, check test setup and/or bsu test set.

9. Measure CLEAR B-N pulse at A14-27 (3F8A). If pulse is not present, proceed to next step.

10. Measure ADDRESS-P pulse at A15-35 (2H3A). If ADDRESS is present, proceed to step 11. If ADDRESS is not present, check the test setup and/or the bsu test set.

11. Measure ADDRESS-P at A14-12 (2H3A). If not present, replace card A14.

12. Measure ADDCMPRI-N at A12-16 (2G2A). If present, proceed to step 16. If not present, proceed to step 13.

13. Measure ADB-N and ADB9X-P. If present, replace card A12. If not present, proceed to step 14.

14. Check setting of ADDRESS SELECT switches on special project bsu/biu and bsu test set.

15. Measure a positive level at output of address compare exclusive or circuit at area 2H5A through 2F5D. Replace card A10.

NOTE

The signal appears in steps 18, 19, 21, and 22 once each time BEAM SET switch is pressed while in INTRG RUN mode of test set. Therefore, a scope trace flash appears on the oscilloscope each time the BEAM SET switch is pressed.

16. At test set change ADDRESS SELECT switch to 111110001. Press INTRG and RUN switches.

17. Measure ADDCMPR2-N at A12-20 (2G2B). If signal is not present replace card A12. If signal is present, proceed to next step.

18. Measure REQUEST-N pulse at A13-10 (3E5B). If pulse is present, proceed to step 25. If not present, proceed to next step.

19. Measure REQUEST-P at A14-20 (3D2A). If present, replace card A13. If not present, proceed to next step.

20. Measure ADDR-P at A14-3 (3D7B). If the signal is not present, proceed to step 24. If the signal is present, proceed to next step.

21. Measure PQST-P at A4-13 (3D4B). If pulse is not present, proceed to next step. If pulse is present, replace card A13 or A14.

22. Measure BEAMSET-N at A4-9. If pulse is not present, replace card A1. If pulse is still not present, Investigate BEAM SET switch A22916. If pulse is present, proceed to next step.

23. Measure DELAY-P at A5-34 (3B7A). If pulse is present, replace card A12 or A6. If pulse is not present, replace card A5.

24. Measure PWRUPCLR-N level at A14-21 (3C7A). If level is low (0 volt), replace card A14. If level is high, return to step 18 and recheck steps.

25. At the bsu test set, momentarily press DATA ENTER, REPLY and RUN switches.

If BAND A and AZIMUTH 000 appears on the bsu/biu, proceed to next step. If not, proceed to step 28.

26. At bsu test set change BAND to B and AZIMUTH to 123. If BAND B and AZIMUTH 123 appear on bsu/biu, proceed to step 27. If not, proceed to step 28.

27. At bsu test set, change BAND to C and AZIMUTH to 246. If BAND C and AZIMUTH 246 appear on bsu/biu, the bsu/biu is operational. If not, proceed to step 28.

28. Switch oscilloscope sync to internal; measure DATA pulse at A3-14 (2E3A). If pulse is present, proceed to next step. If pulse is not present, check test setup and/or bsu test set.

29. Momentarily press INTG and RUN switches on test set. Measure PRESET-P at A3-10 (2E2A) when pressing BEAM SELECT. (See note following step 15.) If pulse is not present, replace card A3. If pulse is present, proceed to next step.

30. Measure SR CLEAR at A3-21 (2E6B). If pulse is not present, replace card A3. If pulse Is present, proceed to next step.

31. Measure BT10 through BT14 while pressing BEAM SELECT switch. If positive levels at appropriate outputs are not observed, replace card Al. If level is observed, proceed to next step.

5-12. Special Project Bsu/Biu Troubleshooting. (See table 5-4 and figure 5-3.)

The special project bsu/biu troubleshooting table (table 5-4) provides symptoms normally observed while troubleshooting the special project bsu/biu. Accompanying the symptom are a number of causes and the probable remedy. If replacement of the indicated replaceable component does not repair the unit, normal signal tracing procedures must be performed. If a defective circuit card is located, refer to Card Repair Manual IM 32-5895-239-15 for repair procedures. Parts location is provided in figure 5-3.

Table 5-4. Special Project Bsu/Biu Troubleshooting

Step	Symptom	Cause	Remedy
1	Band and azimuth data is consistently incorrect	1. Input/output register defective	Replace circuit card A9, A12, or A13
		2. Display register defective	Replace circuit card A11, A4, A12, A13, or A14
2	Band and azimuth data is not updated	1. Clock or clear signal defective	Replace circuit card A14 or A13
		2. Strobe signal not generated	Replace circuit card A12, A13, or A14
3	MODE SELECT or FAULT indicator does not work	1. Bulb defective	Replace bulb
		2. Driver defective	Replace circuit card A7, A5, A6, or A12
4	Entire bsu/biu does not work, or works eratically	1. Power supply voltage incorrect	Adjust power supply output voltage
		2. Line fuse open	Replace line fuse

Table 5-4. Special Project Bsu/Biu Troubleshooting (Continued)

Step	Symptom	Cause	Remedy
		3. Power supply defective	Repair power supply
		4. Power Switch defective	Replace power switch S5
5	No AZIMUTH BEAM SELECT switch causes a change in status	1. Load-register circuit defective	Replace circuit card A4, A1, A14, A12, or A15
		2. Register defective	Replace circuit card A3, A8, A5, or A6
		3. Inverter defective	Replace circuit card A14
		4. Diode matrix defective	Replace circuit card A2, A1, or A16
6	No switches, except LAMP TEST and POWER ON cause a change in status	1. Address recognition logic defective	Replace circuit card A11, A14, or A12
		2. Request logic defective	Replace circuit card A4, A13, or A6
7	Some band or azimuth data is consistently incorrect	1. Input/output register defective	Replace circuit card A9 or A15
		2. Display register defective	Replace circuit card A11 or A15
		3. Display defective	Replace defective display

5-13. Substation Performance Tests. (See figures 5-4, 5-5, and 7-6.)

The substation operational tests provide procedural steps to localize a faulty circuit card in the substation. Test setup is shown in figure 5-4. Carefully perform the steps in sequence. When a defective card is located, refer to Card Repair Manual IM 32-5895-239-15 for repair procedures. Parts location is shown in figure 5-5. Logic is shown in figure 7-6.

a. At the digital test station, connect the substation to the bsu/biu test set and bsu/biu as shown in figure 5-4.

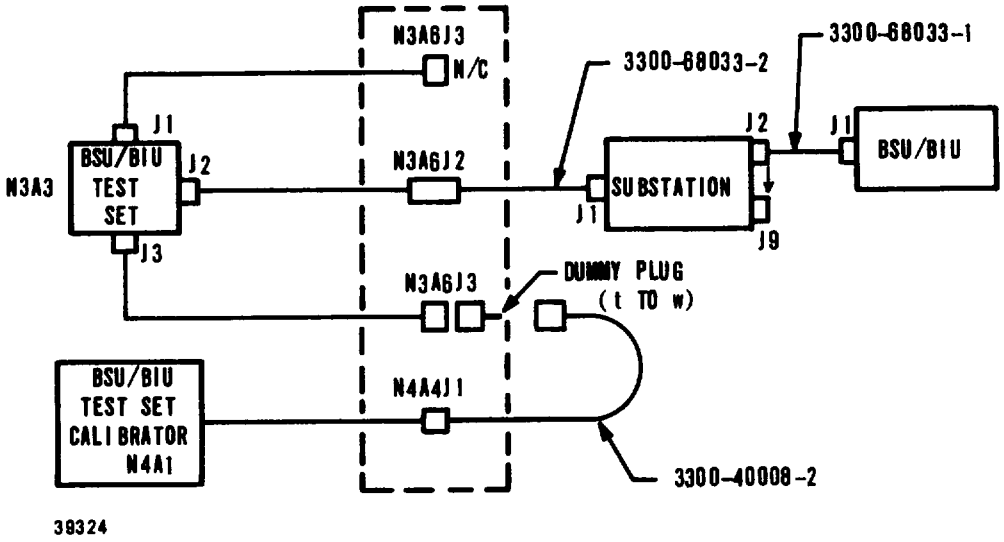

Figure 5-4. Substation Test Setup

b. At the substation, perform the following.

1. Set POWER switch to ON.

2. Measure 5 +0.5 volts dc with less than 50 millivolts ripple between pin 60 of card A3 and chassis ground. If voltage is out of tolerance, perform power supply troubleshooting defined in paragraph 5-16.

c. At the bsu/biu, perform the following.

1. Set POWER switch to ON.
2. Remove switch cover and set ADDRESS SELECT switches to 010101010.
3. Momentarily press RCVR 1 switch.

d. At the bsu/test set, perform the following.

1. Set POWER switch to ON.
2. Set ADDRESS SELECT switches to 010101010.
3. Set BSU-SUB/STA switch to SUB/STA.
4. Momentarily press ADDRESS ENTER switch.
5. Set RCVR I/RCVR 2 switch to RCVR 1.
6. Set BAND switch to A.
7. Set AZIMUTH switches to 010.
8. Set FAULT switch to OFF.
9. Momentarily press INTRG switch.
10. Momentarily press RUN switch.

e. Signal trace the substation as follows.

1. Using the oscilloscope on internal sync, measure CLOCK at A3-50 (IE6A).
2. If CLOCK is present, proceed to step 3. If CLOCK is not present, check test setup.
3. Connect the sync input of the oscilloscope to A3-50 (1E6A) adjust the oscilloscope for external sync.
4. Measure CLOCK at A3-3 (1E2B), A3-31, A3-2, A3-1, A3-5, A3-4, A3-46, and A3-10. If CLOCK is not present at each output, replace card A3. If CLOCK is present at each output, proceed to next step.
5. Measure SERIN at A3-29 (1F4A), A3-26, A3-28, A3-27, A3-22, A3-21, A3-48, and A3-47. If SERIN is not present at each output, replace card A3. If SERIN Is present at each output, proceed to next step.
6. Measure ADDRESS at A3-11 (ID5B). If ADDRESS is not present, replace card A3. If ADDRESS is present, proceed to next step.

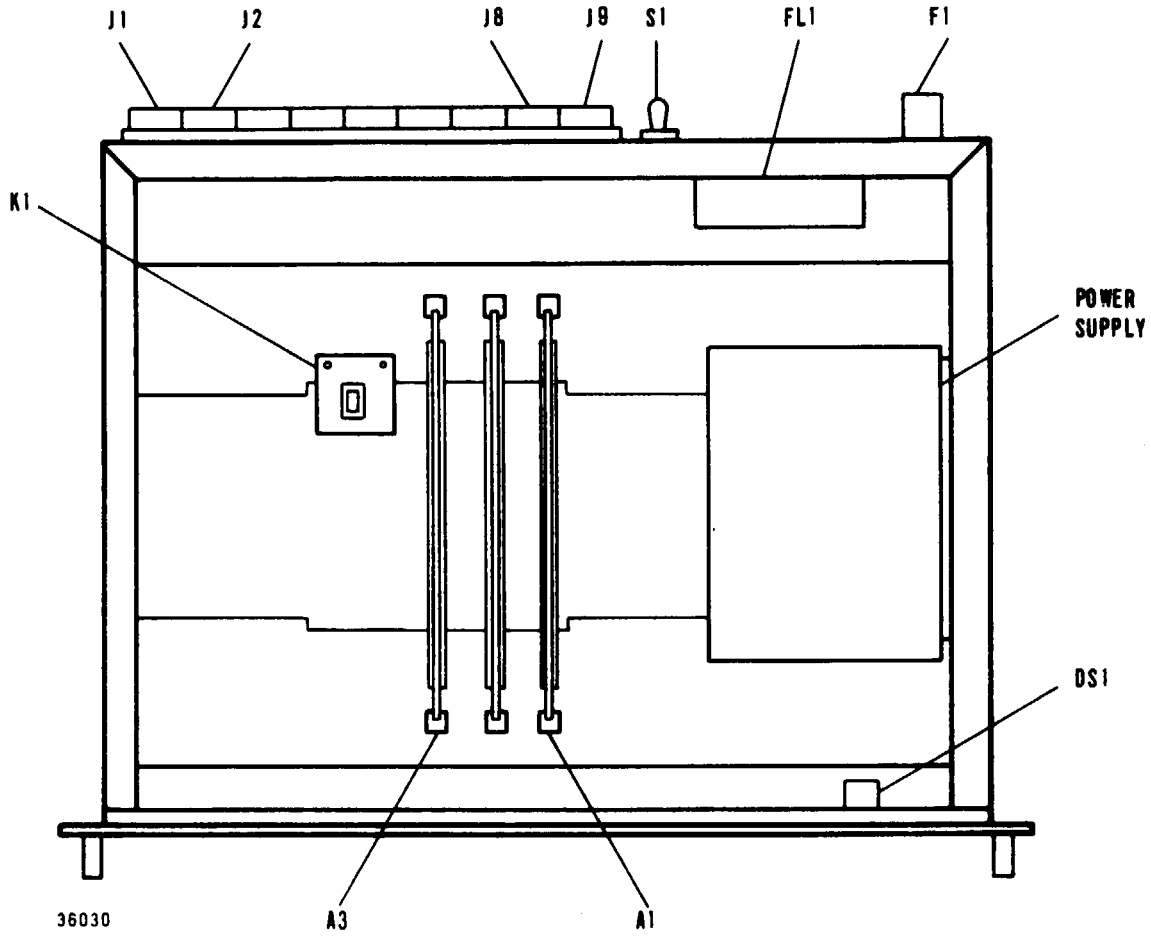

Figure 5-5. Substation Parts Location

7. Measure ADDRESS at A2-5 (1C4A), A2-2, A2-4, A2-3, A2-10, A2-7, A2-14, and A2-11. If ADDRESS is present at each output, replace card A2. If ADDRESS is present at each output, proceed to next step.
8. Measure DATA at A3-9 (1C5A). If DATA is not present, replace card A3. If DATA is present, proceed to next step.
9. Measure DATA at A2-18 (IB4A), A2-17, A2-13, A2-12, A2-9, A2-8, A2-23, and A2-22. If DATA is not present at each output, replace card A2. If DATA is present at each output, proceed to next step.
10. Switch oscilloscope to internal sync; press REPLY and RUN. Measure CLEAR at A3-20 (1D5A). If CLEAR is not present, replace card A3. If CLEAR Is present, proceed to next step.
11. Measure CLEAR at A2-28 (ID4A), A2-27, A2-29, A2-26, A2-24, A2-21, A2-19, and A2-16. If CLEAR is not present at each output, replace card A2. If CLEAR is present, proceed to next step.
12. Press INTRG-R and RUN switches. Measure CLOCK at A1-8 (IG5C), and REQUEST at A1-22 (lH5C) when bsu/biu BEAM SELECT is pressed. If either signal is not present, replace card Al. If all signals are present, proceed to next step.
13. Change test cable to substation jack J3 and repeat step 12.
14. Change test cable to remaining substation jacks (J4 through J9) and repeat step 12 for each jack.
15. Replace dummy plug with patch cable 3300-40008-2 to connect test set to test set calibrator.
16. At test set calibrator set POWER to ON and CLOCK to AUTOMATIC.
17. Adjust scope sweep speed to approximately 1 second per centimeter.
18. Momentarily press test set switches REPLY and RUN and any one of the bsu/ biu BEAM SELECT switches.
19. Measure SEROUT at A125 (IH5B).
20. Reflect step 18 as required to determine signal levels.
21. Replace ADDRESS SELECTION switch cover.

5**-14. Substation Bsu/Biu Troubleshooting**. (See table 5-5 and figure 5-5.)

The substation troubleshooting table provides symptoms normally observed while troubleshooting the substation. Accompanying the symptom are a number of causes and the probable remedy. If replacement of the indicated replaceable component does not repair the unit, normal signal tracing procedures as defined in paragraph 5-13 must be performed. If a defective circuit card is located, refer to Card Repair Manual IM 32-5895-239-15 for repair procedures. Parts location is provided in figure 5-5.

Table 5-5. Substation Troubleshooting

Step	Symptom	Cause	Remedy
1	Computer simulator does not receive one of the substation outputs for any bsu/biu.	Driver defective	Replace circuit card A1.
2	No bsu/biu simulator receives a particular signal from the substation.	Receiver defective	Replace circuit card A3.

Table 5-5. Substation Troubleshooting (Continued)

Step	Symptom	Cause	Remedy
3	One (or only several) bsu/biu does not receive either serial input data or clock signal	Buffer defective	Replace circuit card A3
4	One (or only several) bsu/biu does not receive clear address or data command signal,	Buffer defective	Replace circuit card A2

5-15. Position Scanner Troubleshooting. (See table 5-6 and figures 5-6 and 7-7.)

a. General. Troubleshooting of the position scanner is performed while fixed In place. Repair is limited to replacing faulty circuit cards. Alignment and adjustment is not required. Troubleshooting is accomplished by signal measurement techniques In two operating configurations, free running, and control by the system diagnostic routine. Symptom analysis and repair Is outlined in table 5-6. When a faulty circuit card Is located, refer to the Card Repair Manual IM 32-5895-239-15 for repair and checkout procedures. Parts location is provided in figure 5-6.

Table 5-6. Position Scanner Troubleshooting

Step	Symptom	Cause	Remedy
1	Blocks of bsu/biu are not able to obtain new beam assignments	Address counter faulty	Replace circuit cards A105 and A203
2	Only one bsu/biu is able to obtain beam assignment	Address counter flip-flop faulty	Replace circuit cards A105 and A109
3	A non-requesting bsu/biu receives beam assignment display	Computer data address gates faulty	Replace circuit cards A416, A415, A413, and A210
4	Requesting bsu/biu obtains Incorrect beam assignment display	Computer data storage faulty	Replace circuit cards A119, A104, and A108

Table 5-6. Position Scanner Troubleshooting (Continued)

Step	Symptom	Cause	Remedy
5	Requesting bsu/biu obtains incorrect beam assignment display	Bsu/biu data storage faulty	Replace circuit cards A207, A208, A206, and A108
6 (TP1)	I-MHz (1-microsecond) square wave is not present at A102-26	1-MHz oscillator is faulty	Replace circuit cards A101 and A102
7 (TP2)	I-kHz (I millisecond) square wave is not present at A103-27	Clock decade counter faulty	Replace circuit cards A104, A332, A108, and A103
8 (TP3)	50-kHz (20 microseconds) square wave is not present at A105-27	Clock counter circuit faulty	Replace circuit cards A104 and A105
9 (TP4)	(Phase A)-P (20-microsecond level) signal is not present at A106-57	Phase generator circuit faulty	Replace circuit cards A106, A102, and A107
10 (TP5)	(Phase E)-P (20-microsecond level) signal is not present at A106-21	Phase generator circuit faulty	Replace circuit cards A106, A102, and A107
11 (TP6)	(M9STRBINT)-N (20-microsecond level) not present at A108-28 and A206	Phase A control circuit faulty	Replace circuit cards A109. A105, A103, A102, A108,
12 (TP8)	50-microsecond CLK ENBL signal not present at A116-27	Clock enable gates faulty	Replace circuit cards A114 and A116
13 (TP9)	(CTR CLK)-P signal not present at A110-20	Clock gates faulty	Replace circuit card A110
14 (TPI0)	(REG/CTR RST)-P pulse is not present at A110-8 when 120-volt power is applied	Reset gate faulty	Replace circuit cards A110 and A108
15 (TP11)	(SM 7 CNT)-N level is not present at A110-25 during Phase B time.	SM 7 toggle faulty	Replace circuit cards A110 and A107

Table 5-6. Position Scanner Troubleshooting (Continued)

Step	Symptom	Cause	Remedy
16 (TP12)	BORROW-N level is not present at A201-32 at trailing edge of (SM 7 CNT)-N	Up/downcounter is faulty	Replace circuit cards A201-32, A101, and A206
17 (TP14)	(CLK ENBL 1)-P level is not present at A108-24	Clock enable 1 circuit is faulty	Replace circuit cards A110, A107, and A108
18 (TP15)	(CLK ENBL 2)-P level is not present at A102-46	Clock enable 2 circuit is faulty	Replace circuit cards A110, A107 A109, A105, A16, and A102
19 (TP16)	CLK-1 is not present at A116-32	Clock control I gate is faulty	Replace circuit cards A113, A111, A102, and A106
20 (TP17)	CLK-2 is not present at A111-10	Clock control 2 gate is faulty	Replace circuit cards A113, A111, A114, and A108
21 (TP18)	(V PULSE 2)-P is not present at A103-3	Address gate is faulty	Replace circuit cards A103, A108, and A114
22 (TP19)	(D PULSE 2)-P Is not present at A103-10	Data gate is faulty	Replace circuit cards A103, A108, A110, and A116
23 TP20)	(C PULSE 2)-P is not present at A115-25	Clear gate is faulty	Replace circuit cards A115, A206, A110, and A116

b. Free Running Troubleshooting Procedures. The following troubleshooting procedures are conducted with the position scanner operating in a normal mode, but without regard to any input or output signals. The signals measured are generated as a result of the internal 1-MHz oscillator and the associated circuits. Use an oscilloscope to perform the following.

1. Measure I-MHz OSC at A102-26 (1E6A). If signal is not present, replace card A102 and/or A101.
2. Measure a l-kHz J05X-P signal at A103-27 (1F2A). If not present, replace card A103, A108, and/or A104.
3. Measure 10-kHz CLOCK signals at A332-50, A332-22, A332-46, and A332-47 (1G4B).

If not present, replace card A332.

4. Measure a 20-microsecond square wave signal at A106-56. If not present, replace card A104 and A105.

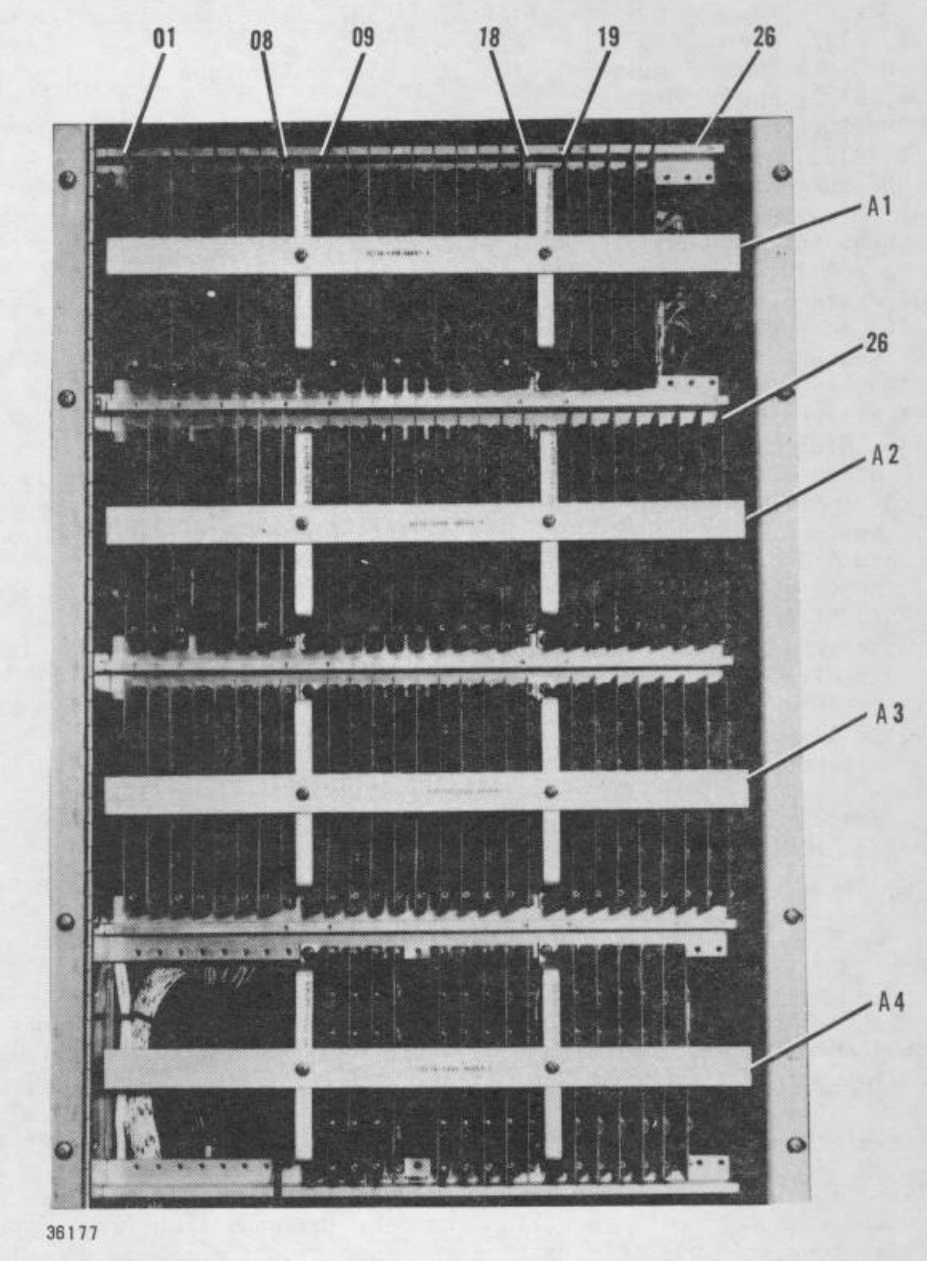

Figure 5-6. Position Scanner 209A1 Parts Location

5. Measure Phase A pulse at A106-57 (1C5A). If signal is not present, replace card A106, A102, and/or A107.

6. Measure Phase E pulse at A106-21 (1C5C). If signal is not present, replace card A106, A102, and/or A107.

7. Measure M9STRB INT at A108-28 (2F4F). If signal is not present, replace card A108, A102, A105, and/or A109.

8. Measure CLOCK ENABLE signal at A116-27 (8E7B). If not present, replace card A116, A114, A112, A111, and/or A105.

9. Measure (CTR CLK) -P signal at A110-20 (8D3A). If signal is not present, replace card A110, A113, A114, A117, and/or A116.

10. Measure (REG/CRT RST) -P at A110-8 (8BSA). If not present, replace card A110, A114, and/or A108.

11. Measure (OA START) -N at A105-9 (3D4A). If not present, replace card A105 and/or A109.

12. Measure BORROW-N at A201-32 (11B4B). If not present, replace card A201, A205, A118, A101, and/or A206.

13. Measure (CLKENBL I) -P pulse at A108-24 (EG7E). If pulse is not present, replace cards A107, A108, and/or A110.

14. Measure (CLK ENBL-2) -P pulse at A102-46 (EF3B). If pulse is not present, replace card A102, A105, A116, A109, and/or A107.

15. Measure 0.5-microsecond pulse at A16-32 (4D6C). If pulse is not present, replace card A113, A111, A102, and/or A116.

16. Measure 0.5-microsecond pulse at A111-10 (4C5B). If pulse is not present, replace card A111, A113, A114, and/or A108.

17. Measure (V PULSE 2) -P at A103-3 (4G2C). If pulse is not present, replace card A103, A108, and/or A114.

18. Measure (V PULSE 1) -P at A115-27 (4G20). If not present, replace card A115.

19. Measure (D PULSE 2) -P at A103-10. If not present, replace cards A103, A116, A110, and/or A108.

20. Measure (C PULSE 2) -P at A115-25. If not present, replace card A115, A206, and/or A110.

NOTE

The System Diagnostic Test Program should be used as a last resort in troubleshooting and isolation. Prior to using this program, obtain permission from the operations officer.

c. Troubleshooting Using System Diaqnostic Test Program. The System Diagnostic Test Program (diagnostic routine) exercises the position scanner using input words which allow signal tracing. The input mode of the diagnostic routine transfers data from the computer to the position scanner. Message transfer is provided once every millisecond. To use this routine the operational program is replaced by the diagnostic routine. Once replaced, the following message is input on the tty.

CYCLE,71,XX,0001010101010101:

where: 71 is position scanner address
XX is any bsu/biu address
16-bit word is as follows:
bit 1 through 3 is no fault
bit 4 is receiver 2
bits 5 and 6 is band B
bit 7 through 16 is 115-degree azimuth
: is end of command.

Once this message is input on the tty, the 16-bit word is transferred to the position scanner by the computer once every millisecond. To terminate the message transfer, input the following message on the tty: END, 71:

d. Troubleshooting Procedures. Perform the following to troubleshoot the position scanner.

1. Obtain permission from the operations officer to replace the operational program.

2. Refer to Technical Manual for Countermeasures Receiving Set, AN/FLR-9(V7) or (V8) (IM 32-5895-231-15 or IM 32-5895-231-15/1) to load the diagnostic routine.

3. Input on the tty the following message.

CYCLE,71,XX,0001010101010101:

NOTE

An oscilloscope is used to make the following measurements.

4. Measure a high level ADEC-P at A206-12 (14F3B). If not present, replace cards A120, A414, A118, and/or A206.

5. Measure AJJED0-P at A116-3 (10D8A). If not present, replace card A415 and/or A116.

6. Measure JJ02-N through JJ1S5-N at A416-59 (10F6A) through A415-8 (10F2A), respectively. If signal is not present, replace appropriate card. (Signal is either an address bit or a data bit, and therefore, should change levels.) 7. Measure XJACK-P at A108-3 (10B7A). If signal Is not present, replace card A108.

8. Measure XJ02A-P through XJ115A-P at A119-59 (10C6A) through A119-6 (100C2A), respectively. If signal is not present, replace appropriate card.

9. Measure (REG CLK) -P at A207-54 (11F6A). If not present, replace A108 and/or A118.

10. Measure (BSU DATA 1) -P at A115-35 (11F2A). If not present, replace card A207, A208, A108, A206, and/or A115. (This is a serial data string.) 11. Measure BSU 1 SERIN through BSU 50 SERIN at A325-29 (12G8A) through A422-23 (12C2A), respectively. If signal is not present, replace appropriate card.

12. Measure AJJ07-P through AJJ15-P (7-bit address word) at A201-28 (1E2A) through A201-43 (1C2A), respectively. If all signals are not present, replace card A201.

13. Measure AJJEDI-P at A120-10 (10D7A). If signal is not present, replace card A120 and/or A415.

14. Measure AJJSTR-P at A116-6 (10D8A). If signal is not present, replace card A116 and/or A411.

15. Measure (SRQ RST) -N at A109-28 (3B5B). If signal is not present, replace card A109.

16. Measure (SCAN ADD 08) -P at A203-24 (2E5A). If signal does not change periodically, replace cards A203, A105, A110, and/or A107.

17. Measure BSU CLEAR at A313-59 (5G8A) and all remaining outputs of this signal. Replace appropriate cards.

18. Measure BSU DATA at A307-59 (7G7A) and all remaining outputs of this signal. Replace appropriate cards.

19. Measure BSU ADD at A301-59 (6G8A) and all remaining outputs of this signal. Replace appropriate cards.

20. Measure BSU CLK at A319-59 (9G8A) and all remaining outputs of this signal. Replace appropriate cards.

21. Measure BSU RQST at A211-59 (13G7A) and all remaining inputs of this signal. Replace appropriate cards.

22. Measure BSU SER 0UT at A233-59 (15H7A) and all remaining inputs of this signal. Replace appropriate cards.

23. Measure BSU CLK R at A217-59 (16G7A) and all remaining inputs of this signal. Replace appropriate cards.

24. Refer to Technical Manual for Countermeasures Receiving Set AN/FLR-9(V7) or (v8) (IM 32-5895-231-15 or IM 32-5895-231-15/1) to load the systems operational program.

5-16. Power Supply Troubleshooting. (See figure 5-7 and table 5-7.) Perform the following steps to set up the power supply unit for troubleshooting.

a. Remove power supply from unit (see paragraph 5-17.d.).

b. Connect a variable line transformer between one ac power line and TB-i.

c. Connect a 5K ohm,)-watt, 10-percent tolerance resistor between TB1-3 and TB1-6.

d. Connect a multimeter between TB1-3 and TB1-6 which is set to measure 5 +0.5 volts dc.

e. Connect the ac power line to a 115-volt ac source.

f. Perform procedures outlined in table 5-7 to troubleshoot the power supply.

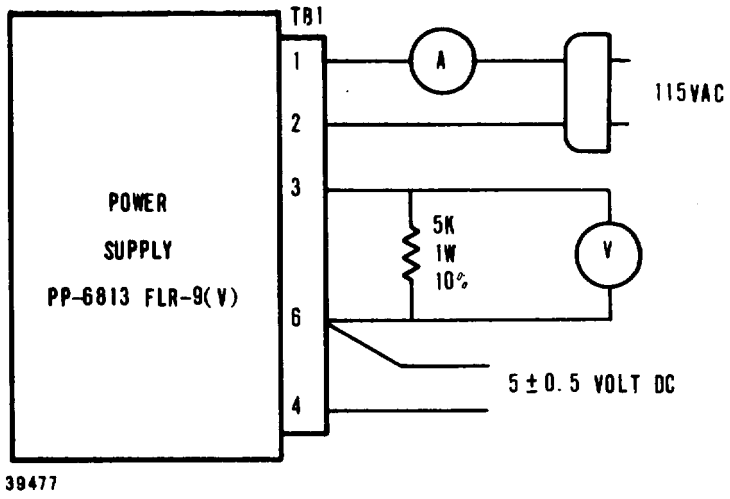

Figure 5-7. Power Supply Test Setup

Table 5-7. Power Supply Troubleshooting

Step	Symptom	Cause	Remedy
1	No output with no input current	1. No ac input voltage	Inspect and correct input ac power
2	Low output or no output with low input current	1. Shorted output	Inspect and correct if short in output is suspected
		2. overvoltage circuit in A2 tripped	Remove ac power for 15 If symptom persists seconds to reset overvoltage circuit replace overvoltage circuit card A2
		3. Defective stage in power supply circuit card A1	Repair power supply circuit card A1
3	Low output or no output with high input current	1. Defective stage in power supply circuit card A1	Locate and replace defective component on circuit card
		2. Defective filter capacitor C1 or C2	Replace defective capacitor
		3. Defective transformer T1	Replace transformer
4	Ripple voltage in excess of 50 millivolts -	1. Defective filter capacitor C1 or C2	Replace defective capacitor
		2. Defective filter in power supply circuit card A1	Repair power supply circuit card

5-17. Repair Procedures.

The following paragraphs contain repair instructions for the intercept group equipments at the general support and depot maintenance level.

a. General Parts Replacement Techniques. The equipments used in the Intercept group are all of modular design and employ the use of solid-state components throughout. This design concept minimizes downtime by providing parts which are easily located and replaced if found to be faulty. Subchassis have major part designations and test points silk screened on the covers and all printed circuit boards are etched engraved with part reference designations. Using this information and the figures in the manual showing the location of components, any part used to construct the equipment can be quickly and easily located. 0nce a circuit card is found to be faulty, refer to the Card Repair Manual IM 32-5895-239-15 for repair procedures pertaining to that particular card.

b. Removal and Installation of Units. The bsu/biu, special project bsu/biu, and the substation are easily removed from the cabinet without observing any special procedures. Be sure to disconnect the cables on the rear panel to avoid damage to the cables and connectors. In the paragraphs which follow, instructions are given for the removal and installation of printed circuit boards and subchassis which make up the bsu/biu special project bsu/biu, and substation.

c. Removal and Installation of Printed Circuit Boards. Printed circuit board modules are removed from the chassis using a circuit board puller. Do not force or pry the printed circuit boards during removal or installation.

d. Removal of Power Supply. (See figure 5-8.) Perform the following steps to remove the power supply from the unit.

1. Remove ac power from the unit.
2. Remove both top and bottom covers from the unit.

CAUTION
Support the power supply case to prevent damage from fall.

3. Remove four screws from the bottom of the power supply case.
4. Ensure that the Ground, Ac Line, Ac Ground, + 0ut, and - 0ut leads are adequately marked to aid in replacing the power supply case.
5. Tilt the power supply case and remove the following leads.
   (a) Ground
   (b) Ac Line
   (c) Ac Ground
   (d) + 0ut
   (e) - 0ut
6. Remove the power supply from the unit.

WARNING
Discharge filter capacitors C1, C2, C6, and C4.

e. Replacement of Power Supply. (See figure 5-8.) Perform the following steps to replace the power supply case in the unit.

1. Connect the following leads to appropriate terminals on the power supply case.
   (a) - 0ut
   (b) + 0ut
   (c) Ac Ground
   (d) Ac Line
   (e) Ground
2. Place power supply case in the unit and attach case to unit using four 6-32 screws.
3. Replace both top and bottom covers to the unit.

f. Power Supply Disassembly. Perform the following steps to disassemble the power supply unit.

1. Remove black lead from (-).
2. Remove red lead from (+).
3. Remove both gray leads from transformer TI.
4. Remove two screws from the mounting base of Q7.
5. Pull Q7 from transistor socket and remove from power supply.
6. Remove two screws from the mounting base of Q8.

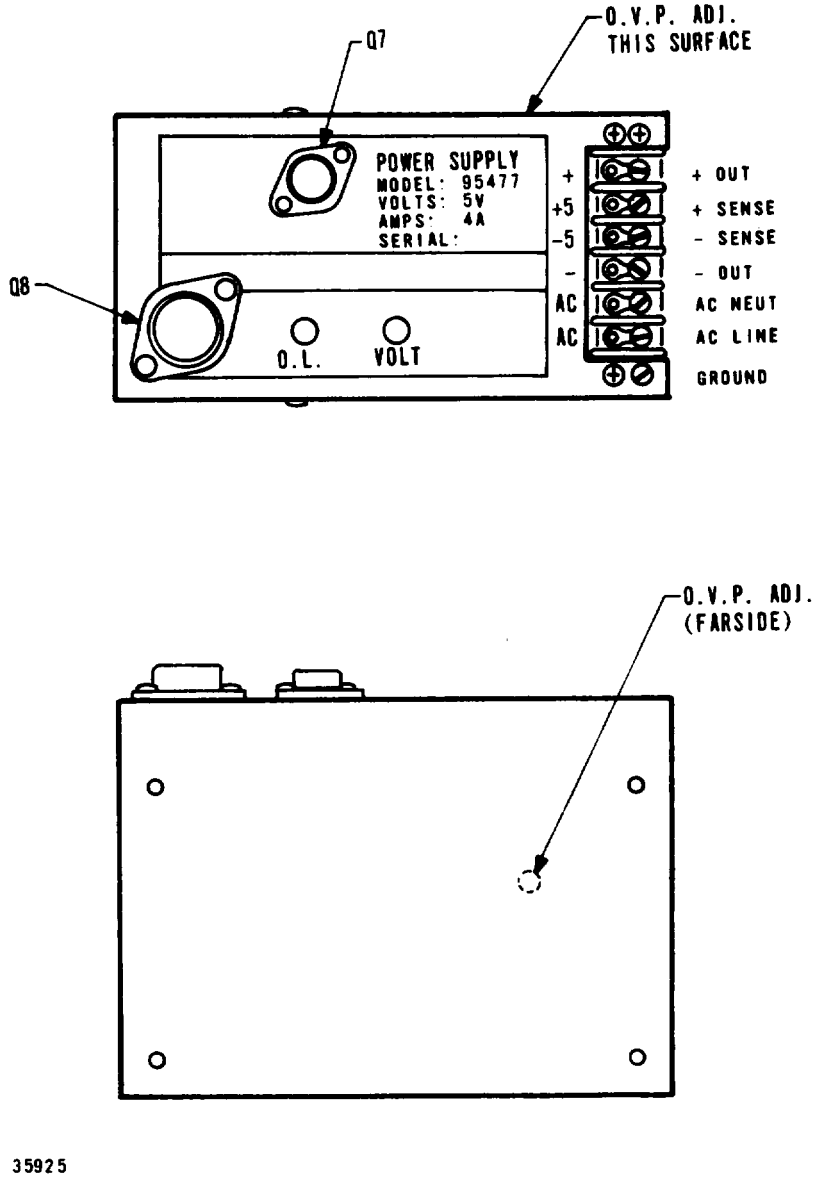

Figure 5-8. Power Supply Parts Location

7. Pull Q8 from transistor socket and remove from power supply.
8. Remove black and red leads from C1 9. Remove C1 from power supply.
10. Remove black and red leads from C2.
11. Remove C2 from power supply.
12. Remove orange lead from rectifier circuit.
13. Remove four screws securing the power supply circuit card to the case and remove the circuit card.
14. Remove two screws from side of the power supply case securing the overvoltage circuit card to the case.
15. Remove the overvoltage circuit card from the case.

NOTE

The overvoltage circuit card is a non-maintenance item which may be destroyed upon removal.

g. Power Supply Assembly. Perform the following steps to assemble the power supply.

1. Place the overvoltage circuit card in the power supply case and attach using two 6-32 screws.
2. Place the power supply circuit card in the power supply case and attach using four 6-32 screws.
3. Attach orange lead to center terminal of rectifier circuit.
4. Place C2 in holder clamp.
5. Attach black lead to negative terminal and red lead to positive terminal of C2.
6. Place C1 in holder clamp.
7. Attach black lead to negative terminal and red lead to positive terminal of C1.
8. Insert Q8 in transistor socket and attach using two 8-32 screws.
9. Insert Q7 in transistor socket and attach using two 8-32 screws.
10. Attach a gray lead to the two transformer terminals.
11. Attach red lead to (+).
12. Attach black lead to (-).

h. Fiber 0ptic Display Disassembly. (See figure 5-9.)

1. To replace lamps in the fiber optic display assembly, perform the following:

(a) Prior to removing the fiber optic display from the unit, remove the lamp assembly by pulling outward on the flanged area.
(b) Remove the two contact block retaining screws and remove the block.
(c) Replace defective lamps and replace the contact block. Tighten screws to pull contact block against lamp assembly.

2. To replace the lamp driver chip, perform the following steps.

(a) Set POWER switch to OFF.
(b) Carefully mark the wires connected to the fiber optic display jack to facilitate reassembly and remove the wires.
(c) Remove the panel fiber optic display assembly from the unit panel by grasping the fiber optic unit at the rear of the assembly and working the unit out through the front panel.
(d) Bend up the maintenance release retaining clips (4 each).
(e) Pull the driver housing from the unit.

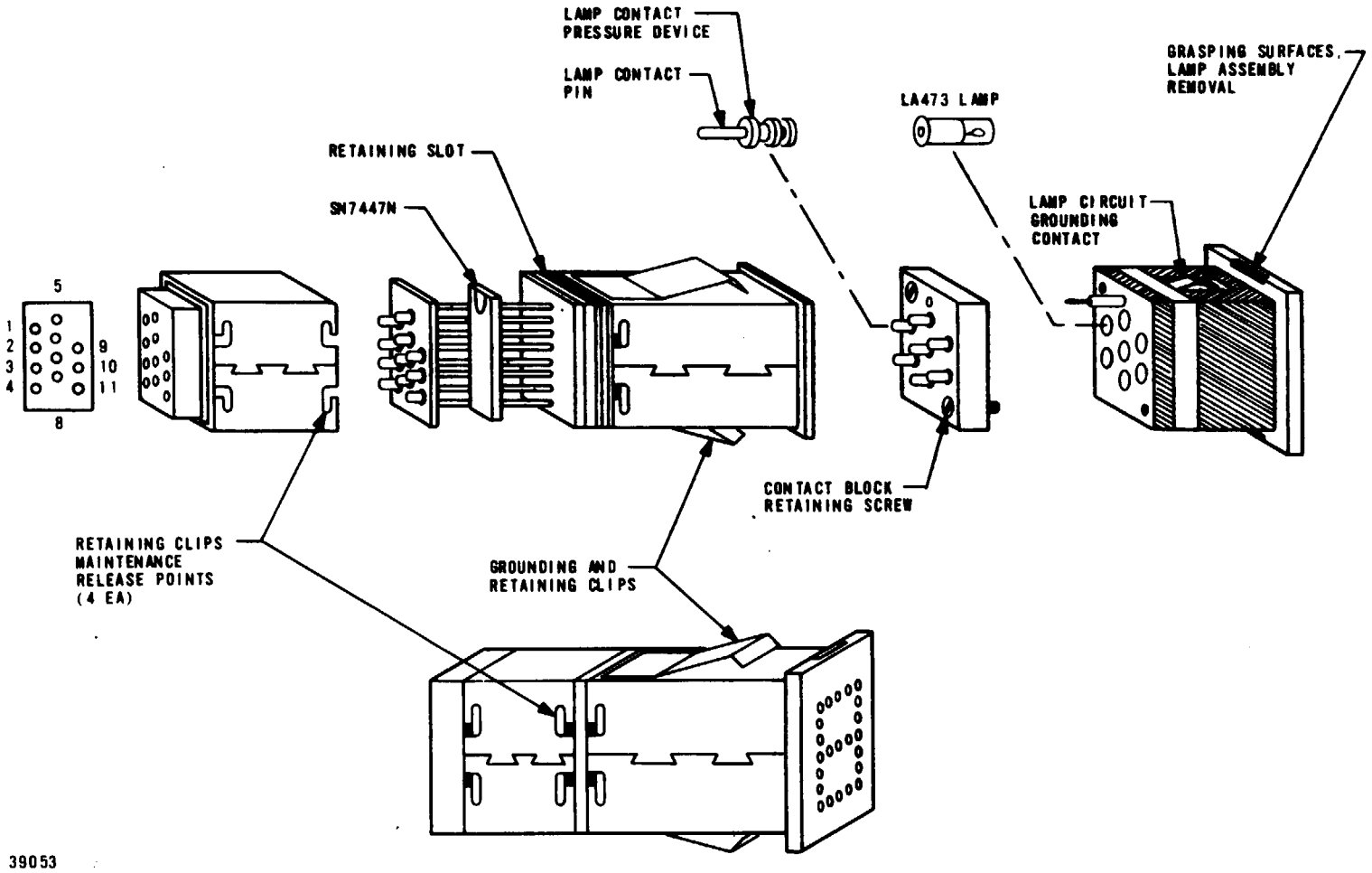

Figure 5-9. Fiber Optics Display Assembly Drawing

(f) Using a solder sucker and soldering iron, remove solder from each lamp driver chip connector.
(9) Remove the chip.
(h) Replace the chip and resolder each connection.
(i) 0bserving guide pin number 5, replace the driver housing.
(j) Bend down the retaining clips.
(k) Insert the fiber optic unit in the front panel by firmly seating the unit from the front.
(I) Carefully replace the wires in the fiber optic display jacks.

5-18. Alignment and Adjustment.

Alignment and adjustment procedures for equipment within the intercept group is limited to the adjustment of the power supplies in each unit. Perform the following steps to adjust the power supply.

a. Remove top cover from the equipment.
b. Connect the ac power card from the unit to 115-volt ac outlet.
c. Set POWER switch to 0N.
d. Use a Hewlett-Packard, Model 410C, Electronic Voltmeter to measure 5 ± 0.5- volts dc between + and - terminals of the power supply.
e. Adjust the power supply VOLT control (R14) for a 5 ± 0.5-volt dc meter reading.
f. Replace the top cover.

5-19. Minimum Performance Standards. (See table 5-8.)

Minimum performance standards for the intercept group equipment are contained in table 5-8.

Table 5-8. Minimum Performance Standards.

Step	Test Equipment	Procedure	Minimum Acceptable Performance
1	Bsu/biu	1. Press RCVR 1 2. Press a BEAM SELECT switch to select a band A rf signal	BAND and AZIMUTH display selected band and azimuth and selected signal is heard on associated receiver number 1
2	Bsu/biu	1. Press RCVR 2 2. Press a BEAM SELECT switch to select a band B rf signal	BAND and AZIMUTH display selected band and azimuth a and selected signal is heard on associated receiver number 2
3	Bsu/biu	1. Press RCVR 1	1. RCVR 1 lamp lights 2. BAND and AZIMUTH display the receiver 1 signal azimuth and band

Table 5-8. Minimum Performance Standards (Continued)'

Step	Test Equipment	Procedure	Minimum Acceptable Performance
4	Bsu/biu	1. Press BEAM SELECT switch to select a band C rf signal	BAND and AZIMUTH display selected band and azimuth and selected signal is heard on associated receiver number 1
5	Special Project Bsu/biu	Press 1. M0N BEAM 2. BAND SELECT A 3. BEAM SELECT DEGREES to select a known rf signal	BAND and AZIMUTH display selected band and azimuth and selected signal is heard on associated receiver

SECTION VI

DEPOT INSPECTION STANDARDS

6-1. Scope.

This section contains optimum performance standards for the bsu/biu, special project bsu/biu, substation, and power supply. Tests outlined in this section should be performed after repair of the three listed equipments has been accomplished.

6-2. Tests (See table 6-1.)

A list of tests to be performed to ensure optimum performance of equipment within the intercept group and the test equipment Involved Is listed in table 6-1. The special project bsu/biu and position scanner are fixed in place equipment and have no requirements for depot inspection standards.

Table 6-1. Inspection Standard Tests

Equipment	Test	Test Equipment
Bsu/Biu	Bsu/Biu Operational Test	Test Set Beam Selection-Identification Unit TS-3283/FLR-9(V)
Special Project Bsu/Biu	Special Project Bsu/Biu Operational Test	Cable, Multiconductor 3300-68033-1
Substation	Substation Operational Test	Test Set Beam Selection Identification Unit TS-3283/FLR-9(V) Cable Multiconductor 3300-68033-2

6-3. Test Equipment.

Test equipment required to perform the operational tests are listed in table 5-2.

6-4. Bsu/Biu Operational Test.

Means to determine the operational performance of a bsu/biu are provided in the following procedures. Satisfactory results of each procedural step must be obtained, if not refer to maintenance section procedures for troubleshooting and repair.

a. Connect the bsu/biu to the Test Set Beam Selection-Identification Unit TS-3283/FLR-9(V) (bsu test set) as shown in figure 5-1.
b. Set POWER switch on each unit to ON and allow a 15-minute warmup.
c. At the bsu/biu observe a figure 8 display in the BAND and AZIMUTH display lamp while holding the DISPLAY LAMP TEST pressed.
d. At the bsu test set perform the following:
    1. Remove switch cover and set ADDRESS SELECT switches to 010101010.
    2. Set BSU/SUB/STA switch to BSU.
    3. Set RCVR 1-RCVR 2 switch to RCVR 1.
    4. Set BAND switch to A.

5. Set AZIMUTH to 000.
6. Set FAULT switch to OFF.
7. Momentarily press test set ADDRESS ENTER and DATA ENTER switches.

e. At the bsu/biu perform the following:
1. Set ADDRESS SELECTION switches to 010101010.
2. Press RCVR 1 switch and observe that lamp lights.

f. Perform the following at the indicated unit:
1. Momentarily press test set REPLY and RUN switches.
2. At the bsu test set, set BAND switch to A, B, then to C. Observe an A, a B, and then a C displayed on the bsu/biu BEAM indicator.
3. Rotate the bsu test set AZIMUTH hundreds, tens, and digits controls through a full cycle. Observe identical display on the bsu/biu AZIMUTH indicator as the controls are cycled.
4. Press test set INTRG and RUN switches.
5. Press the bsu/biu BEAM 1 switch. Observe the bsu test set BEAM SELECT lamp indicates identical beam as switch is set.
6. Repeat steps 4. and 5. using all bsu/biu BEAM SELECT switches.
7. Repeat step 4. and then press NO BEAM and then FAULT switches on bsu/biu. Observe that the NO BEAM and FAULT lamps light on the bsu test set.
8. Set RCVR l-RCVR 2 switch on bsu test set to RCVR 2. Press bsu/biu RCVR 2 and BEAM 1 switches. Observe RCVR 2 lamp light on both units and beam I on test set lights.
9. Set ADDRESS SELECT switches on both units to 101010101.
10. Set bsu test set AZIMUTH switch to another setting.
11. Press test set REPLY and RUN switches. Observe new azimuth indication on bsu/biu.
12. Replace ADDRESS SELECTION switch cover.

6-5. Special Project Bsu/Biu Operational Test.

Means to determine the operational performance of the special project bsu/biu are provided in the following procedures. Satisfactory results of each procedural step must be observed; if not, refer to maintenance section procedures for troubleshooting and repair. Connect the equipment to the bsu test set as shown in figure 5-1.

a. At Bsu test set position.
1. BSU-SUB/STA to BSU
2. RCVR 1-RCVR 2 to RCVR 1
3. FAULT to OFF
4. ADDRESS SELECT to 111110000
5. Press ADDRESS and DATA ENTER switches.
6. Press REPLY and RUN switches.

b. Rotate test set BAND and AZIMUTH switches and observe identical reading on bsu/biu BAND and AZIMUTH Indicators.

c. At bsu/biu press:
1. BEAM CLEAR
2. SECTOR BEAM
3. BAND SELECT B
4. BEAM SELECT DEGREES 010
5. BEAM SET.

d. Observe that the test set BEAM SELECTED 16 lamp, RCVR 1, and INTRG lamps light.
e. Index address on test set by 1 (111110001) and press RUN twice.
f. Observe the test set BEAM SELECTED 8 lamp lights.
g. Repeat step c. using MON BEAM, BAND SELECT A and BEAM SELECT DEGREES 123.
h. Repeat step d. observing the number 3 lamp lights.

i. Repeat step e. observing the number 2 lamp lights.
j. Repeat step c. using OMNIBEAM, BAND SELECT C and BEAM SELECT DEGREES 156.
k. Observe the test set FAULT and RCVR 2 lamp light.
l. Repeat step e. observing the number 18 lamp light.
m. Repeat step c. using MON BEAM, BAND SELECT A and BEAM SELECT DEGREES 789.
n. Observe the test set 9 lamp and RCVR 1 lamp light.
o. Repeat step e. observing the number 7 lamp light.
p. Repeat step c. using MON BEAM, BAND SELECT A and BEAM SELECT DEGREES 124.
q. Observe the test set 4 lamp and RCVR 1 lamp lights.
r. Repeat step e. observing the number 2 lamp light.

6-6. Substation Operational Tests.

The operational performance of a substation is determined by coupling signals through the substation to a bsu/biu and observing the indications on the bsu/biu. To perform this test connect the substation to a bsu/biu and a bsu test set as shown in figure 5-4. Once connected to the test equipment, perform the steps outlined in paragraph 6-4 for the bsu/biu.

GLOSSARY

A

A/D - Analog-to-digital.

ANTENNA ARRAY - Circular disposed antenna elements tuned to a particular band of frequencies.

ANTENNA ELEMENT - A single element used in an antenna array.

ASCII - American Standard code for information interchange (See LEC Leap Assembler Manual).

ASR - Automatic send/receive.

AZIMUTH - Angular direction clockwise from true north.

B

BCD - Binary coded decimal in which lines are weighted 8, 4, 2, and 1.

BEAM ASSIGNMENT TABLE - A table contained In the computer program which defines rf beams available to a radio receiver as selected by a bsu/biu.

BEAMFORMER - A device which forms a directional broadband rf signal.

BLOCKING - Inhibiting use of paths between Al and A2 or A2 and A3 switch matrix submatrices.

BOOTSTRAP - Simple initial computer routine which enables the computer to initiate loading of larger program from an external device.

BORESIGHT ELEMENT - Antenna element to the right of (even elements) or on (odd elements) the received radio beam center line.

BSU/BIU - Beam select unit/Beam Identification unit.

BUFFER - Circuit which stores data or provides load isolation for signal lines.

C

CABLE SCANNER - Multiplexer which routes input signals to the computer.

CARD FILE - Assembly containing circuit cards, card jacks and interconnecting wiring.

CCD - Cyclic coded decimal in which the bits change in segments of one each per word.

CENTRAL BUILDING - Building located in center of antenna array.

CPU - Central processing unit; the computer minus Input/output accessories.

COUPLING - Connection of the same rf input beam to two or more receivers that are connected to the output ports in a common A3 submatrix.

D

DECOUPLING - Use of STAGE REMOVED command to clear switch map table of paths of receivers who are coupled to the same faulty rf beam In the A3 submatrix to allow the operator to obtain an alternate path to the receiver.

DECODER - Circuit for conversion between numerical systems (such as bcd to decimal).

DFG - Direction finding group

DIAGNOSTIC ROUTINE - Special computer program which senses and defines faults.

DIRECTIONAL COUPLER - Passive device which provides low Impedance In the desired direction and high Impedance In all other directions to rf signal inputs.

DIU - Digital interface unit.

DOT-OR - Logical OR function not present in any one circuit; occurs because of the nature of connected outputs from other circuits.

DAUGHTER BOARD - Pcb which mounts on a motherboard.

DUMP - Output computer memory contents to some output device such as a tty.

E

EAI - External address in; computer output signal which enables transfer of address between two computers.

ECI - External command input; computer output signal which enables routing of a command to the computer.

ECO - External command output computer output signal which defines the nature of i/o bus signal.

EDI - External data input; computer output signal which enables routing of data to the computer.

EDO - External data output; computer output signal which defines the nature of i/o bus signal.

EMI - Electromagnetic interference.

ESI - External status input; computer output signal which enables routing of status signal to the computer.

EXCLUSIVE-OR - Logic circuit which produces a high output when one (not more than one) input is high.

G

Goniometer - Rotating device which forms a directional rf beam from received signals.

H

HANDOVER - Occurs when the primary computer relinquishes control of the system to the on-line standby computer.

HEXADECIHAL - The numbering system in the computer program which uses 16 as a radix. The 16 combination of bits in a 4-bit group provides decimal digits of 0 through 9 and A through F.

INTERFACE - Circuits between the computer and other equipment necessary for routing, storage, format/level conversion, or special processing.

INTERRUPT - Causes computer to stop doing a relatively unimportant routine and perform one of higher priority; after interrupt, computer returns to previous task.

I/O - Input and output.

I/O BUS - Computer's connection to external equipment.

I/O BUS SWITCH - Routes signals from/to active computer to/from external devices.

I/O DRIVER RECEIVER - Line driver and signal converter.

IPDC - Internal programmed data channel.

J

J**-K FLIP-FLOP** - Flip-flop which can be operated asynchronously, like an R-S flip-flop, and/or synchronously with a clock, J, and K inputs. The J and K Inputs are sometimes provided with AND gates.

L

LATCH - Storage register.

LEC - Lockheed Electronics Company

LINE DRIVER - Circuit which produces balanced signals in response to single-ended logic signal.

LINE RECEIVER - Circuit which produces a single-ended logic signal in response to a balanced input signal.

LOAD - To enter the program into the computer.

LOGIC - Electronic circuits or groups of circuits designed to make a discrete response to a particular combination of input signal levels.

LOGIC ERROR - Program detects that set is executing at an Illegal location or detects that a cpu controlled parameter is out of limits.

M

MAGNETIC TAPE CONTROLLER - Electrical interface between computer and tape unit; it provides buffering, motion control, and error control.

MATRIX - An array of crosspoints in which any point may be addressed by a system of coordinates.

MATRIX MULTIPLEXER - Multiplexer which routes computer outputs to external equipment.

MCC - Memory control chassis associated with MAC 16 computer.

MDC - Multiplex data channel; a high-speed portion of the computer pdc i/o structure.

MEMORY EXPANSION CHASSIS - Holds all computer memory in excess of 8192 words, and also interface logic circuits.

MONITOR BEAM - A directional beam, selected with automatic selected directivity.

MOTHERBOARD - A circuit card where other circuit cards are physically mounted.

MULTIPLEXER - Signal selector or router which acts as a multiple-pole rotary switch, under external (computer) control.

MUX - Multiplexer.

N

NAND - Circuit which produces a low output only when all inputs are high.

NOR - Circuit which produces a low output when any (one or more) inputs (including all inputs) are high.

O

OLM&T - On-line monitor and test function of the monitor and test group.

OMNIBEAM - A non-directional beam.

OPTICAL ENCODER - Produces a ccd output to define the direction of the goniometer beam.

P

PDC - Programmed data channel; part of computer i/o structure.

PERIPHERAL EQUIPMENT - Equipments interfacing with a single unit of equipment for control or signal application purposes.

PROGRAM - Set of instructions, constraints, and information stored in computer memory which enables a computer to perform a particular task (or series of tasks).

PROGRAM AZIMUTH SHEET - List of beams assigned to a given bsu/biu.

R

REDUNDANT (MUX, CPU, etc) - Energized standby equipment identical to that equipment presently in control.

REED SWITCH MATRIX - Any of three test matrices in the monitor and test group designated matrix A, matrix B, and matrix C and the special project switch matrix.

RFI - Radio frequency interference.

RFSM - Radio frequency switch matrix; a part of the rf matrix group.

ROUTINE - A particular part of an overall program which performs a certain function within the program.

S

SAMPLING MATRIX, OLMST - A reed switch mounting assembly contained as a part of, or all of, an olm&t test matrix designated matrix A, matrix B, or matrix C.

SECTOR BEAM - A directional beam with manually selected directivity.

SINGLE-SHOT - Circuit which produces a single fixed duration pulse In response to an input signal.

SOMC - Supervisory operation maintenance console.

SPECIAL PROJECT BSU/BIU - A beam select unit which selects any bands and beams without requiring a beam assignment table.

STANDBY - The non-controlling computer of the two provided. When on-line, It is continuously accepting data from the primary computer; can assume control Immediately upon request.

SUBMATRIX - Consists of a number of circuit cards, each with multiple inputs and a single output, arranged in such a manner as to provide a two-dimensional (X, Y) array of switchable rf crosspoints.

T

TABLE - An array of data, constraints, or references in the computer program.

TELETYPE CONTROLLER - LEC provided circuit card which provides signal buffering for a teletype under computer control.

TRANSMISSION LINE TUNERS - Coaxial line stretcher.

TSA - Computer program instruction.

TTY - Teletypewriter.

TUNNEL - Underground access between operating building and central building housing connecting cables.

V

VVM - Vector voltmeter.

W

WATCHDOG TIMER - A periodically reset counter which provides an interrupt to the opposite computer if not reset within 150 milliseconds.

X

X-PT - A crosspoint in the switch matrix.

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INDEX (Continued)

INDEX (Continued)

INDEX (Continued)

SECTION VII

MAINTENANCE ILLUSTRATIONS

7-1. Scope.

This section consists of illustrations referenced in sections IV, V, VI, and IX.
The following illustrations are contained within this section:

a. Overall logic diagrams
b. Primary power distribution
c. Dc power distribution.

7-2. Logic Circuit Diagram Labeling. (See figure 7-1.)

Labeling used on the Countermeasures Receiving Set AN/FLR-9 (V7)/V8) logic diagrams is shown in figure 7-1. The labeling identifies the signal origin and destination by use of the diagram sheet number and applicable drawing coordinates. Signal levels (high or low) are identified by use of a P or N following the signal name signifying a high- or low-level signal, respectively. Within each logic symbol, tagging lines are used to specify location of the symbol on the drawing, identification of the integrated circuit, and card location. The example NAND gate, as shown, is located on sheet 2 at coordinates D and 4. The integrated circuit reference designator on this circuit card is U2 and the circuit card is the first card in the third row. In some cases a single alphanumeric digit appears designating the card location. Numbers adjacent to the logic symbols within parentheses identify unique pin numbers on the integrated circuit. Numbers adjacent to the logic symbol which are not within parentheses identify unique circuit card pin numbers.

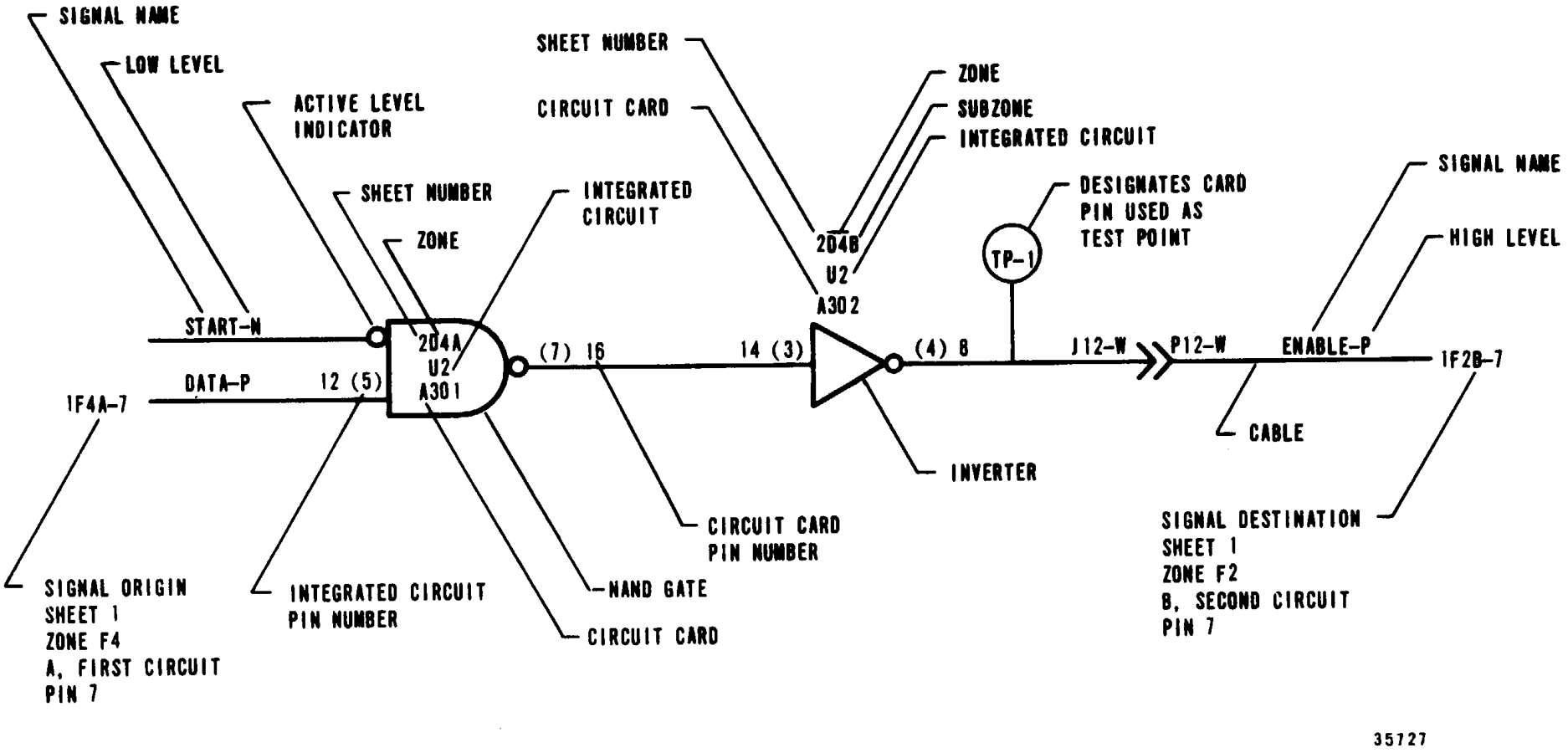

Figure 7-1. Logic Circuit Labeling

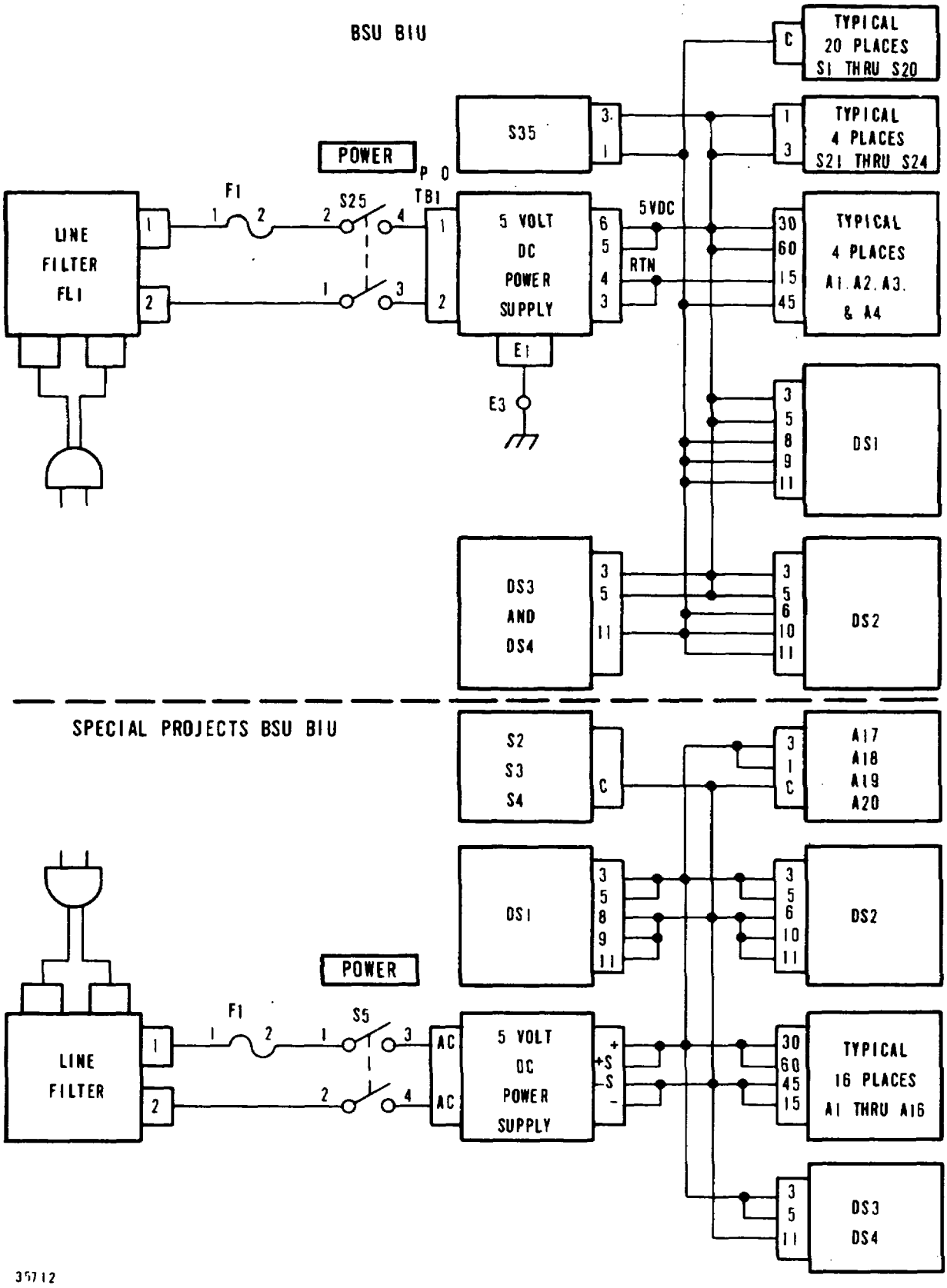

Figure 7-2. Power Distribution, Bsu/Biu and Special Project Bsu/Biu

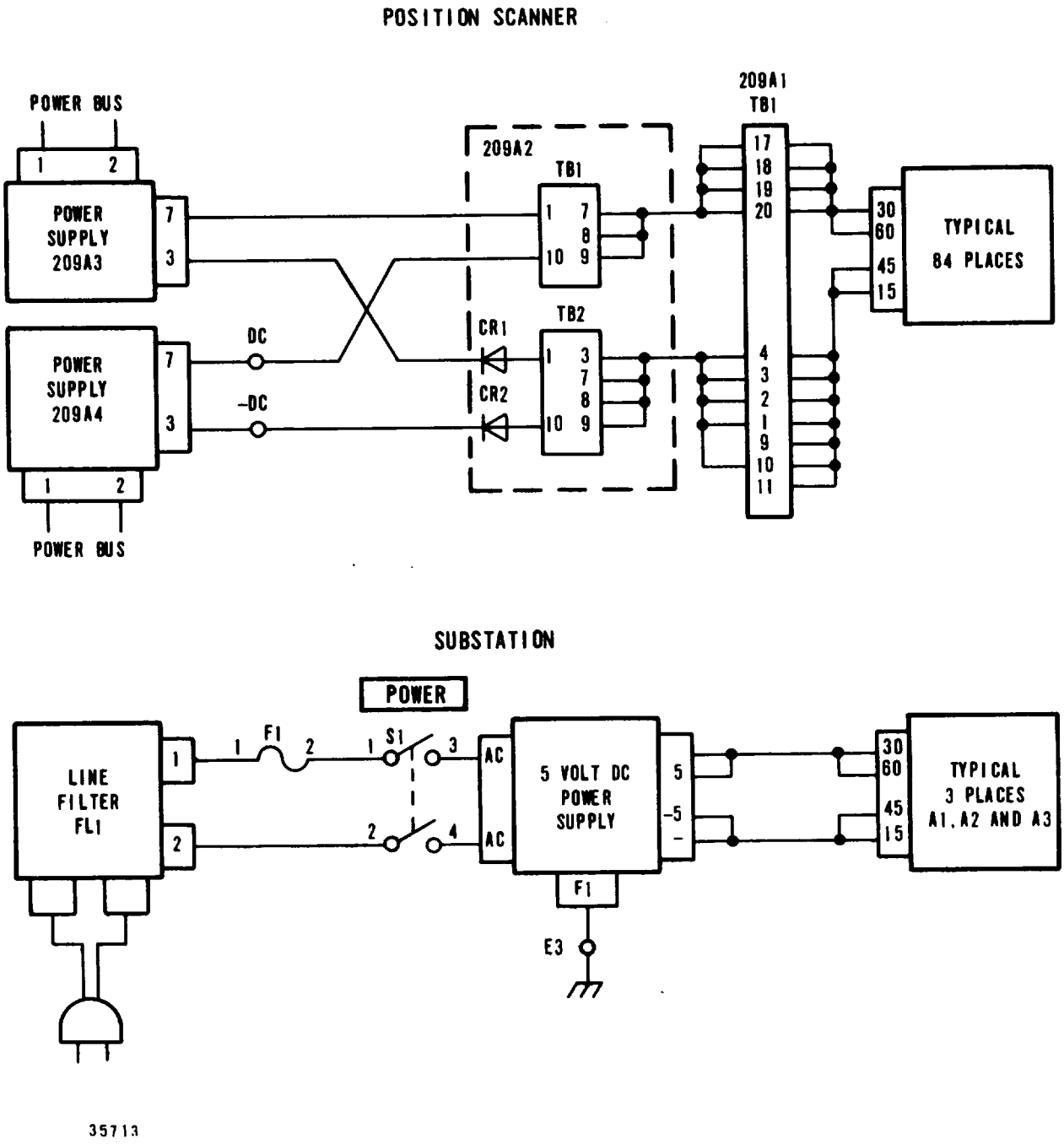

Figure 7-3. Power Distribution, Position Scanner and Substation

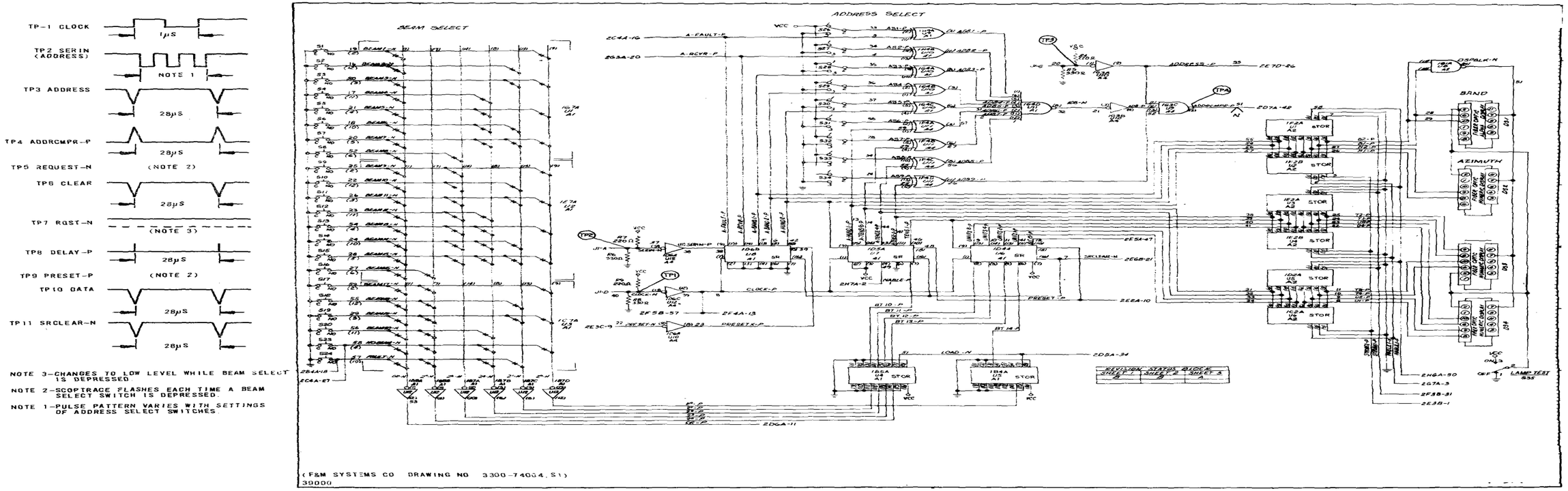

Figure 7-4. Bsu/biu Logic Diagram (Sheet 1 of 4)

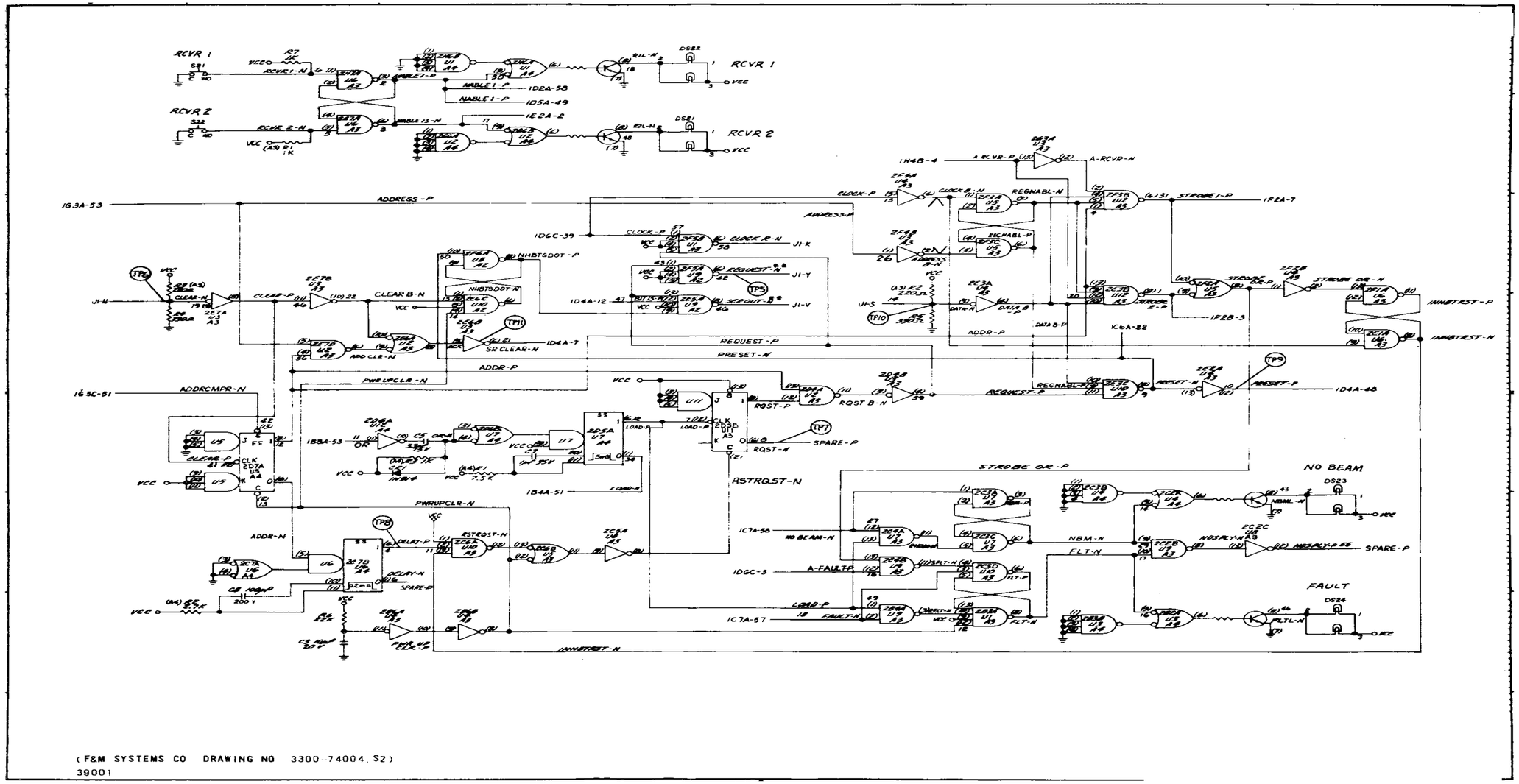

Figure 7-4. Bsu/biu Logic Diagram (Sheet 2 of 4)

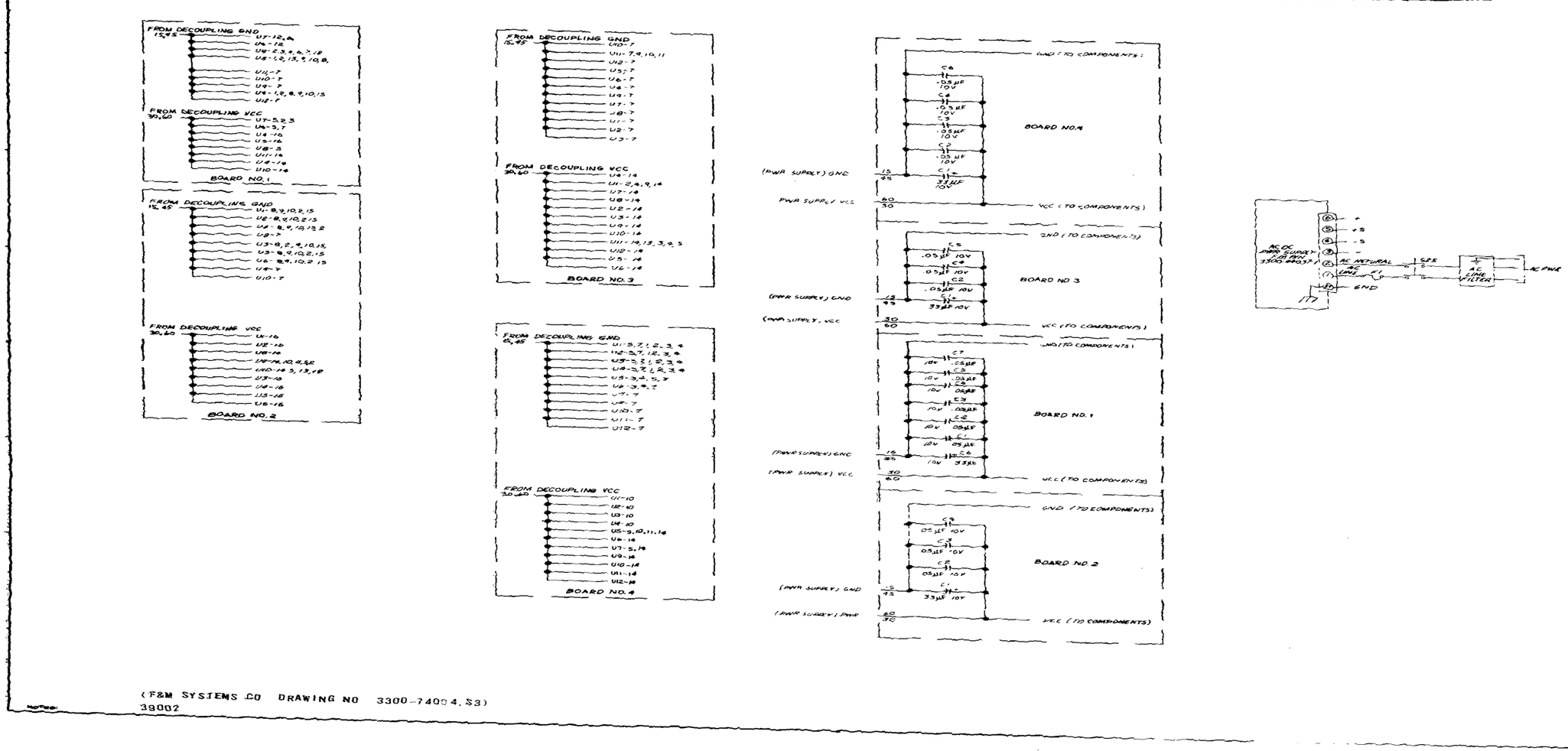

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Figure 7-4. Bsu/biu Logic Diagram (Sheet 3 of 4)

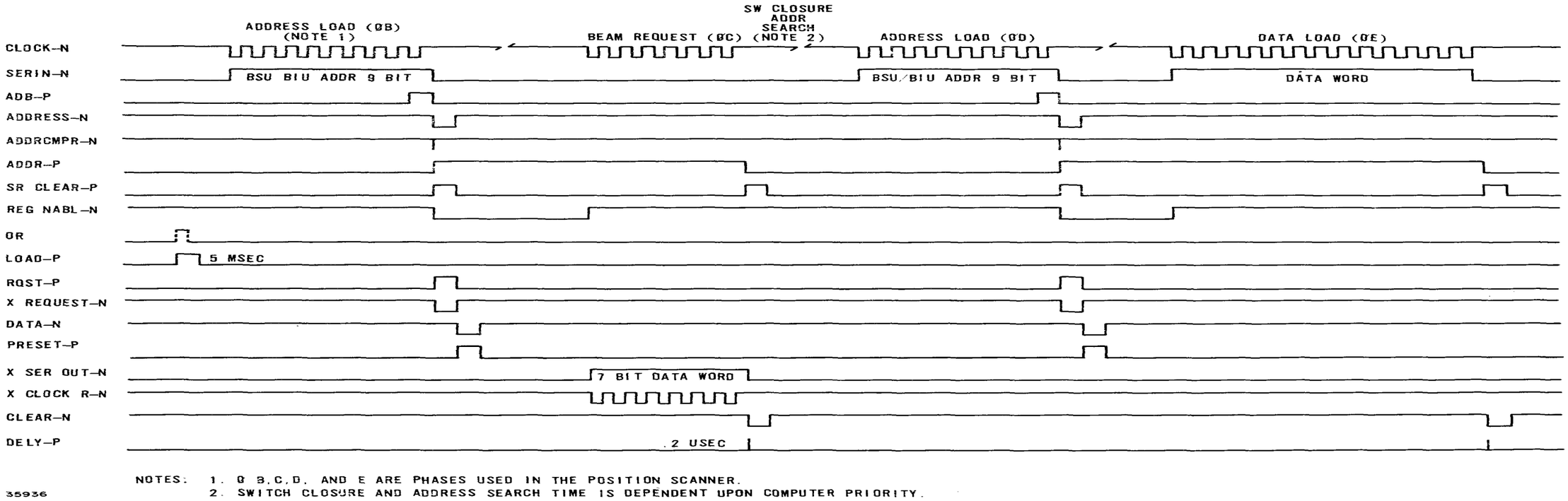


Figure 7-4. Bsu/biu Logic Diagram (Sheet 4 of 4)

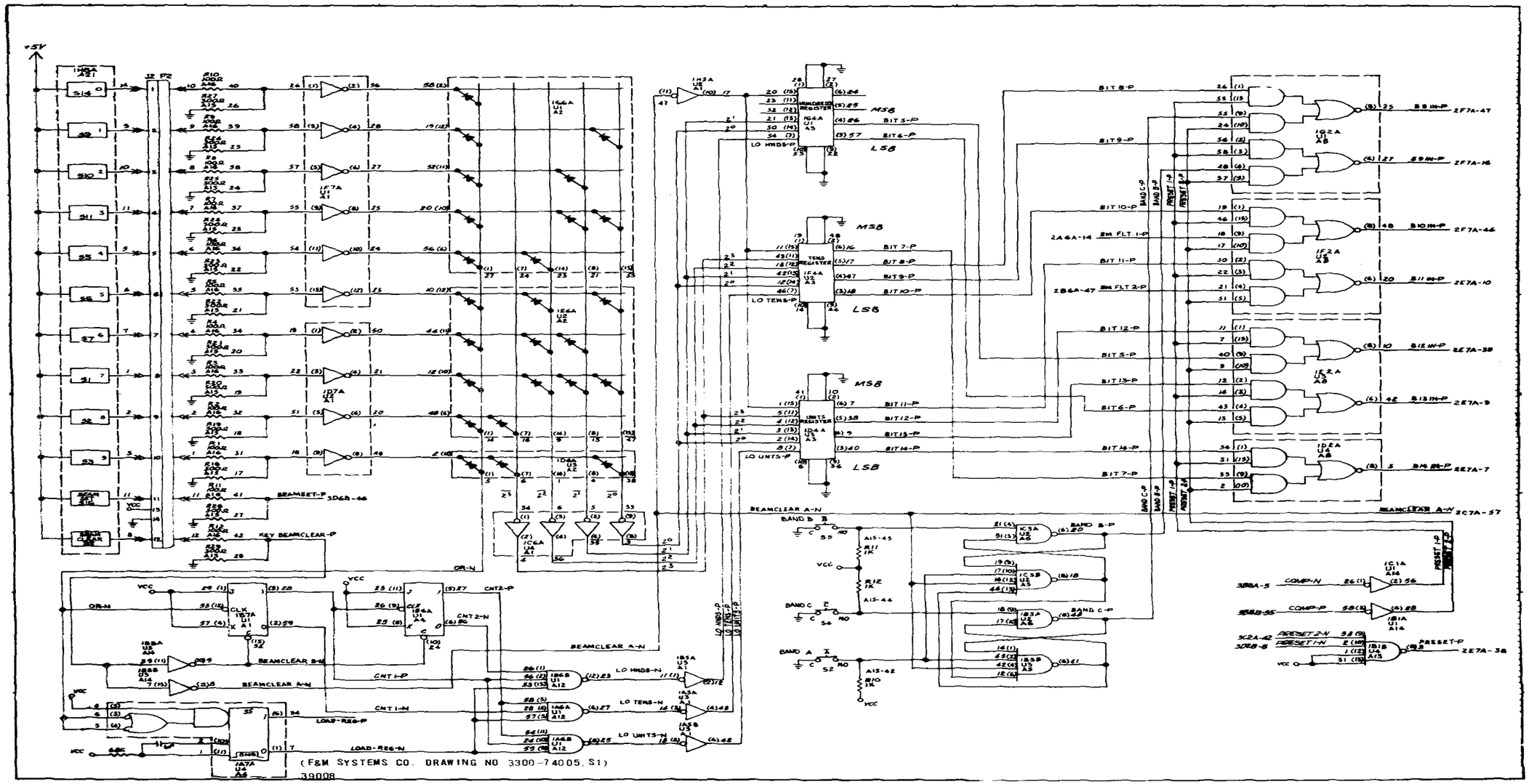


Figure 7-5. Special Projects Bsu/biu Logic Diagram (Sheet 1 of 4)

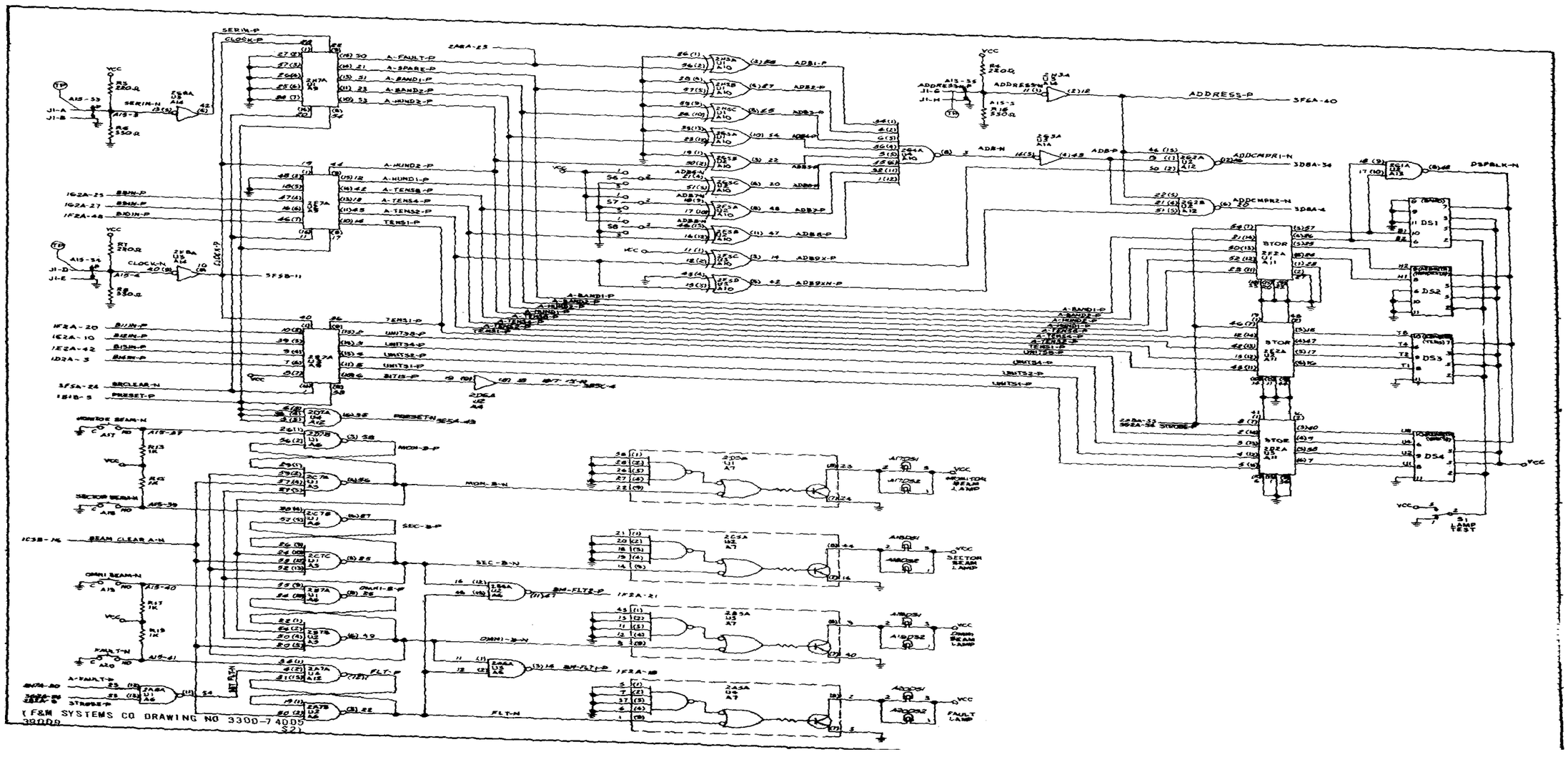


Figure 7-5. Special Projects Bsu/biu Logic Diagram (Sheet 2 of 4)

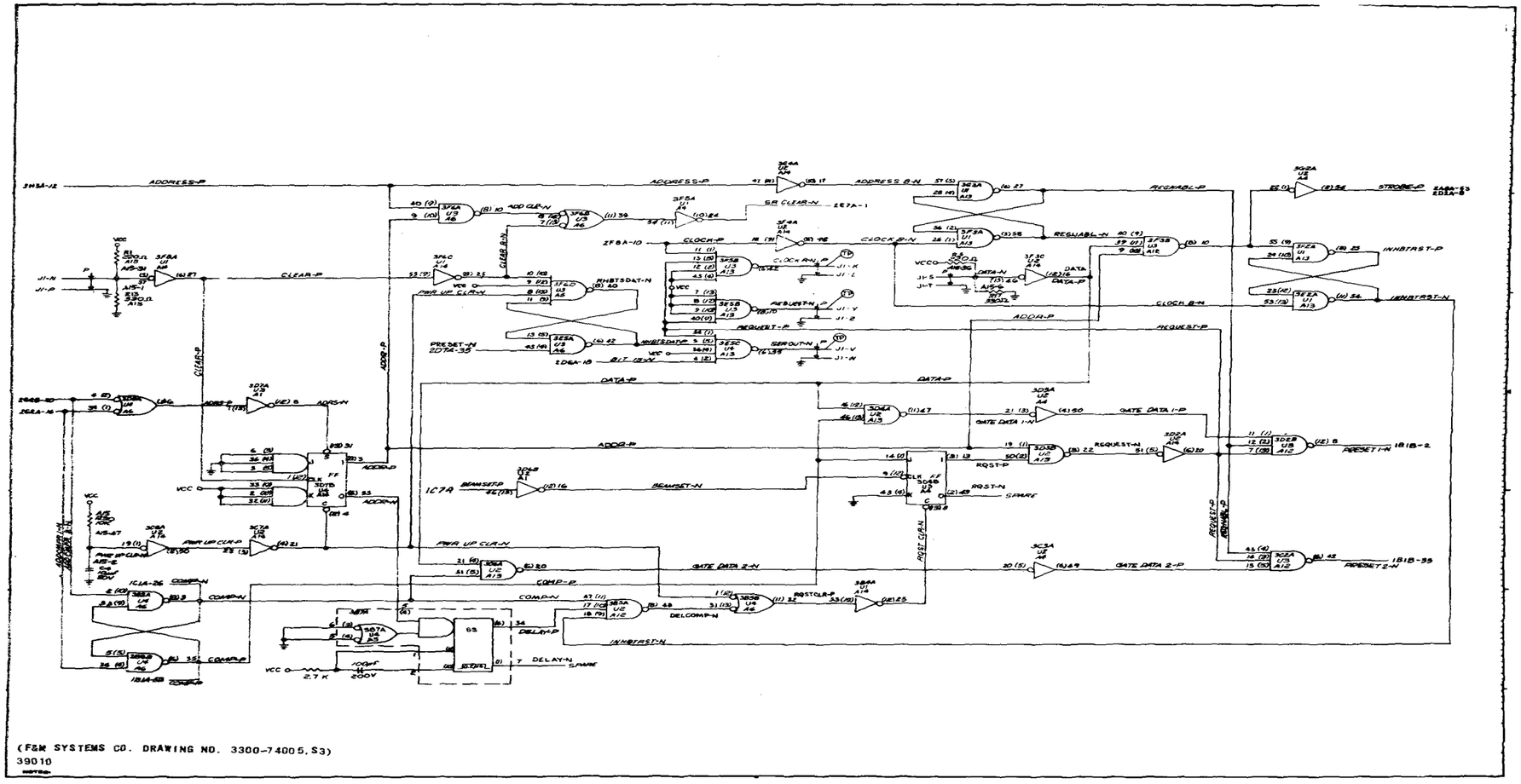
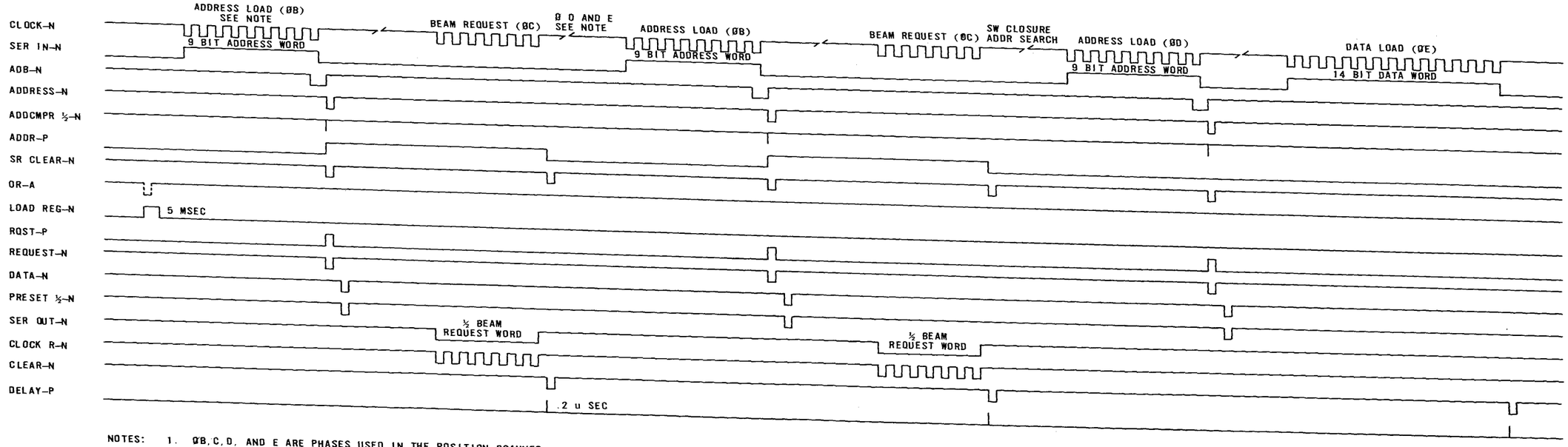


Figure 7-5. Special Projects Bsu/biu Logic Diagram (Sheet 3 of 4)



NOTES:
1. ØB, C, D, AND E ARE PHASES USED IN THE POSITION SCANNER
2. SWITCH CLOSURE AND ADDRESS SEARCH TIME IS DEPENDENT UPON COMPUTER PRIORITY.

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Figure 7-5. Special Projects Bsu/biu Logic Diagram (Sheet 4 of 4)

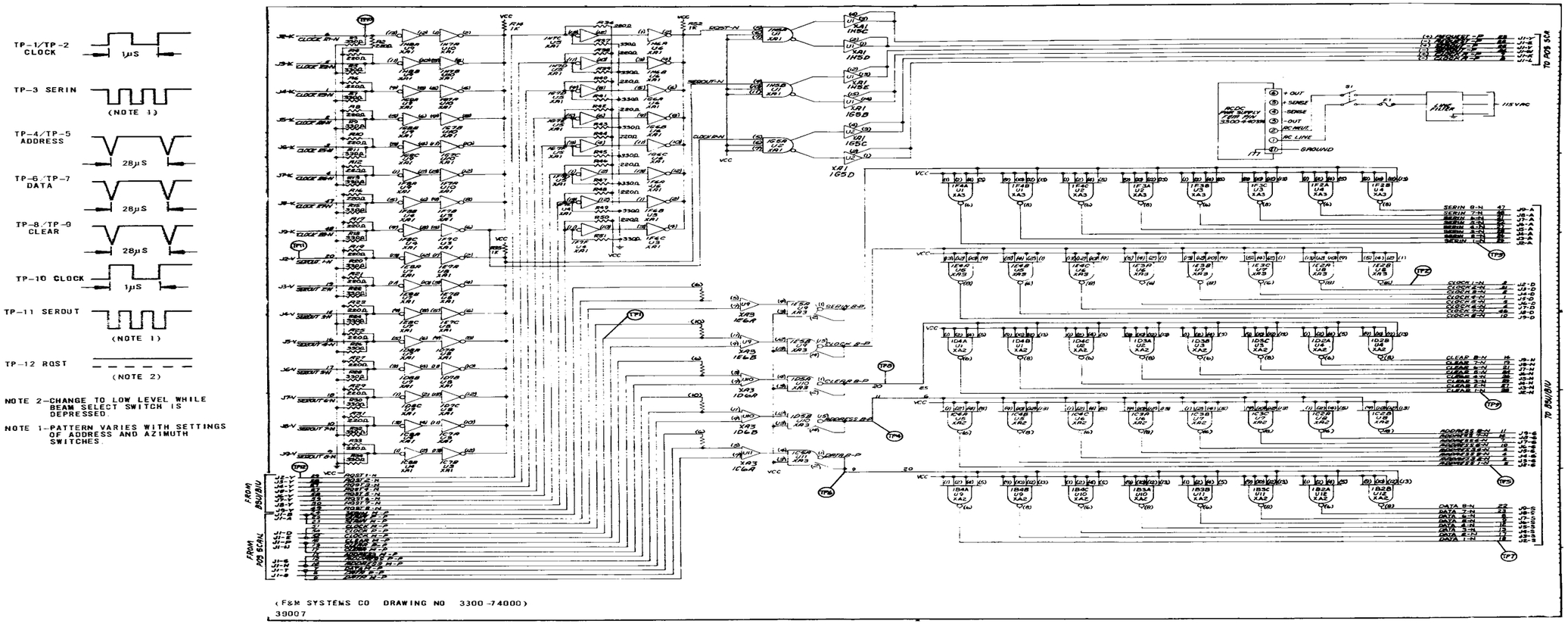


Figure 7-6. Substation Logic Diagram

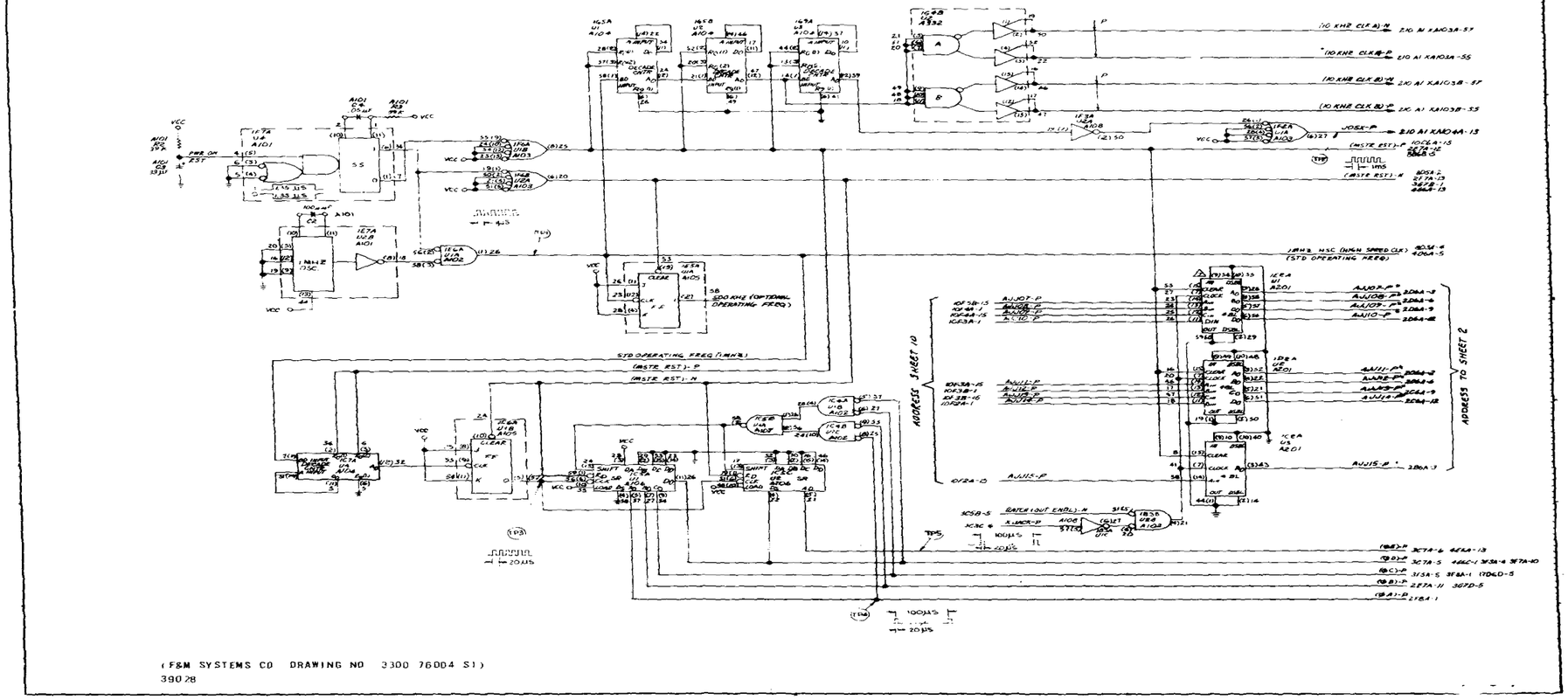


Figure 7-7. Position Scanner Logic Diagram (Sheet 1 of 20)

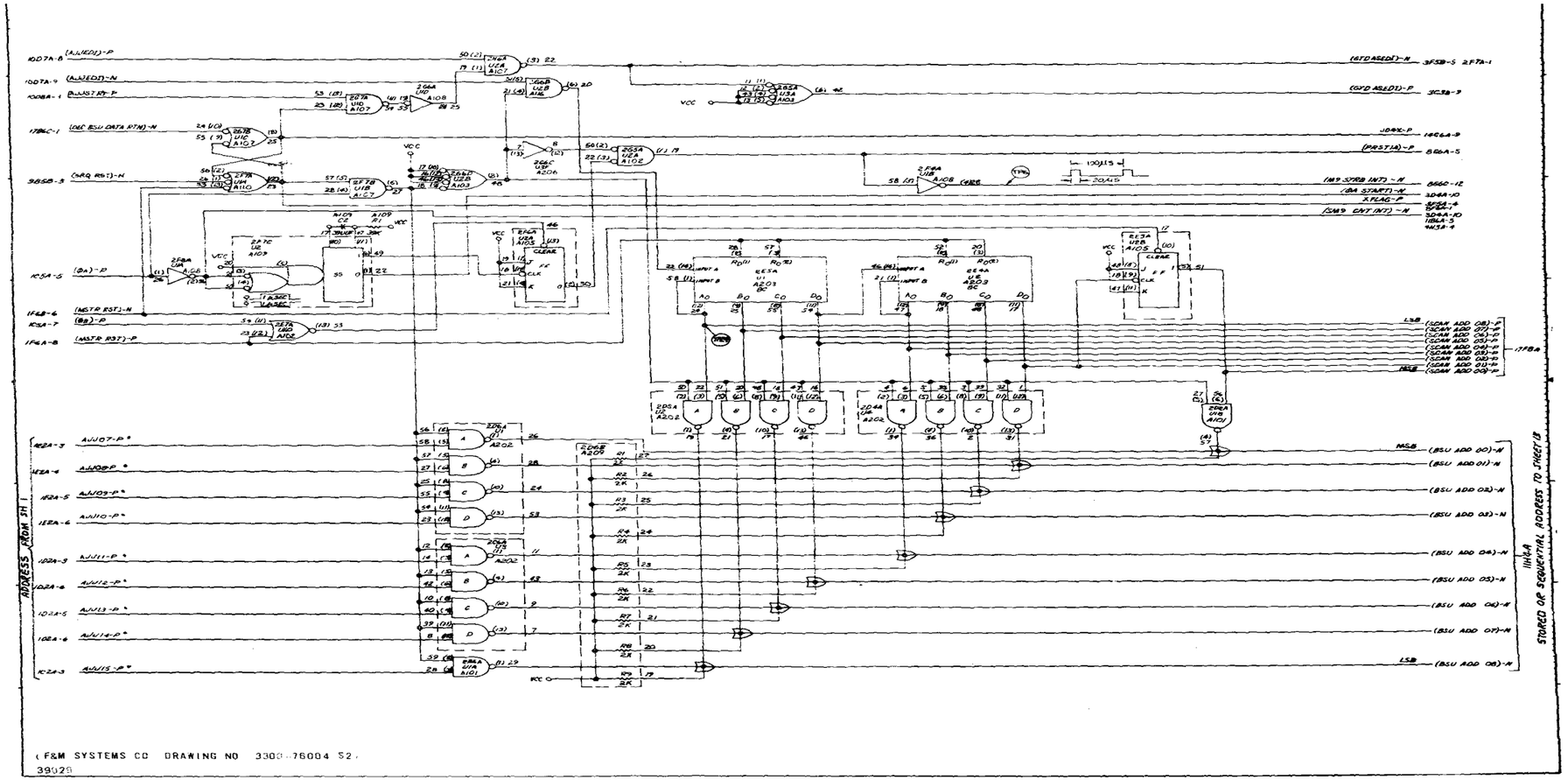


Figure 7-7. Position Scanner Logic Diagram (Sheet 2 of 20)

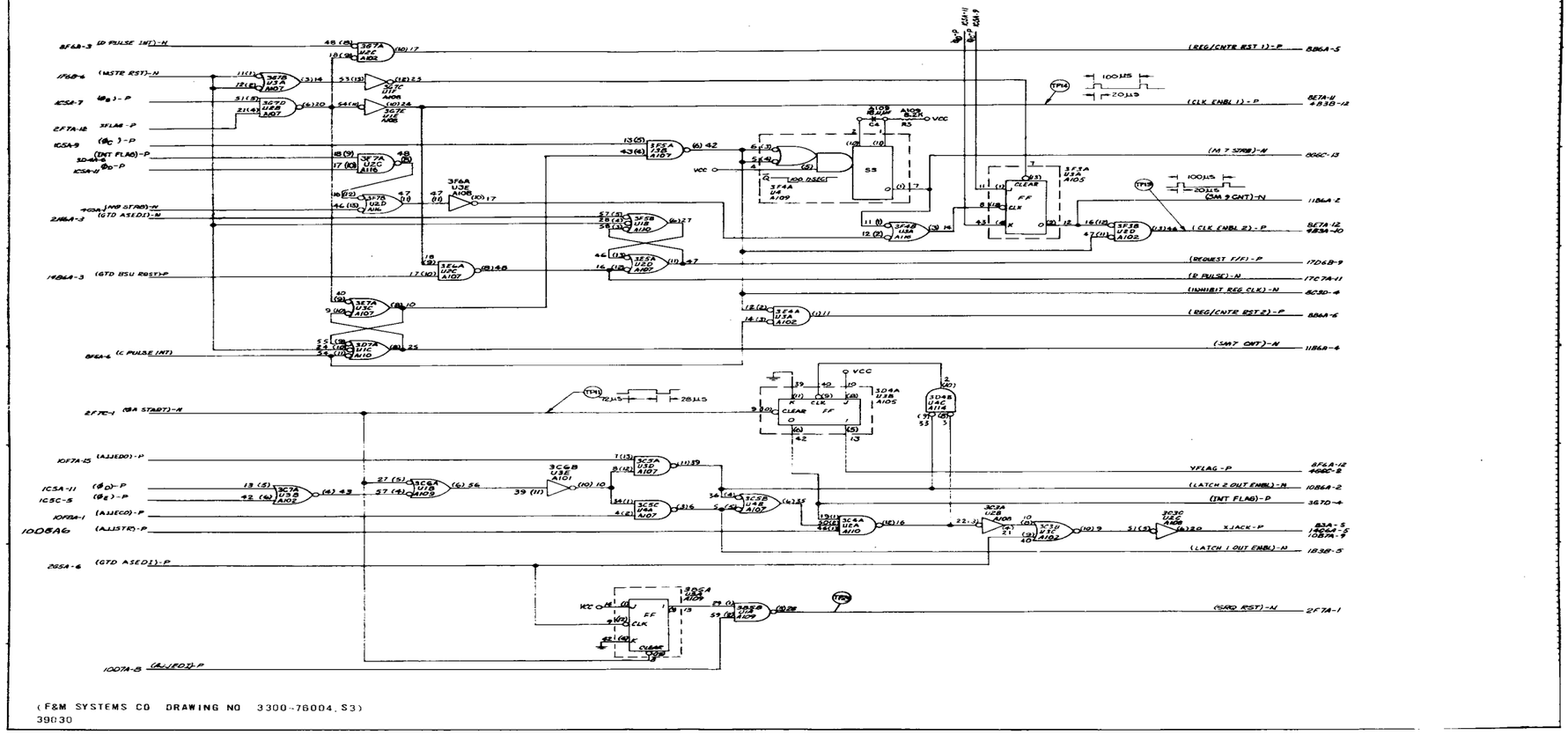


Figure 7-7. Position Scanner Logic Diagram (Sheet 3 of 20)

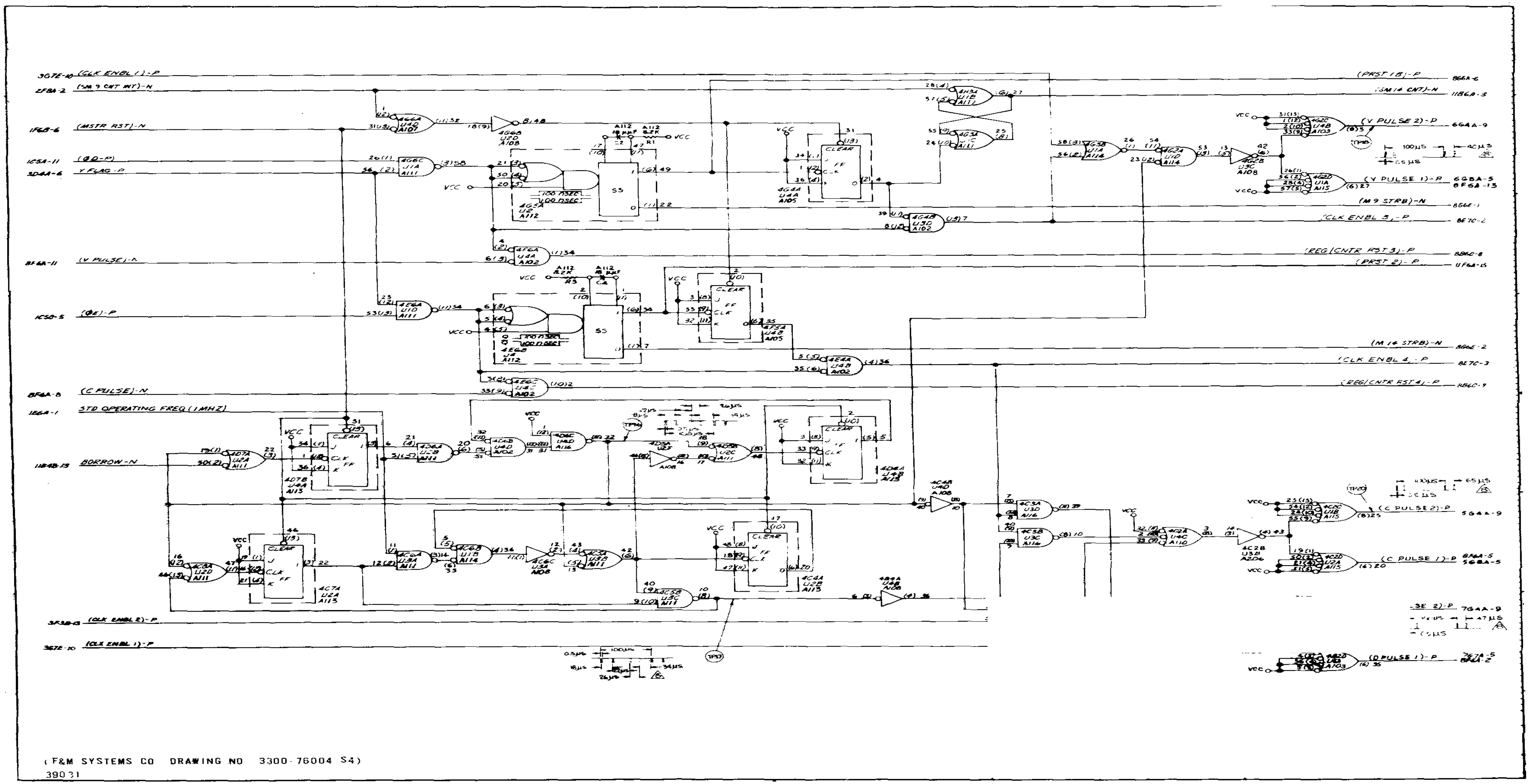


Figure 7-7. Position Scanner Logic Diagram (Sheet 4 of 20)

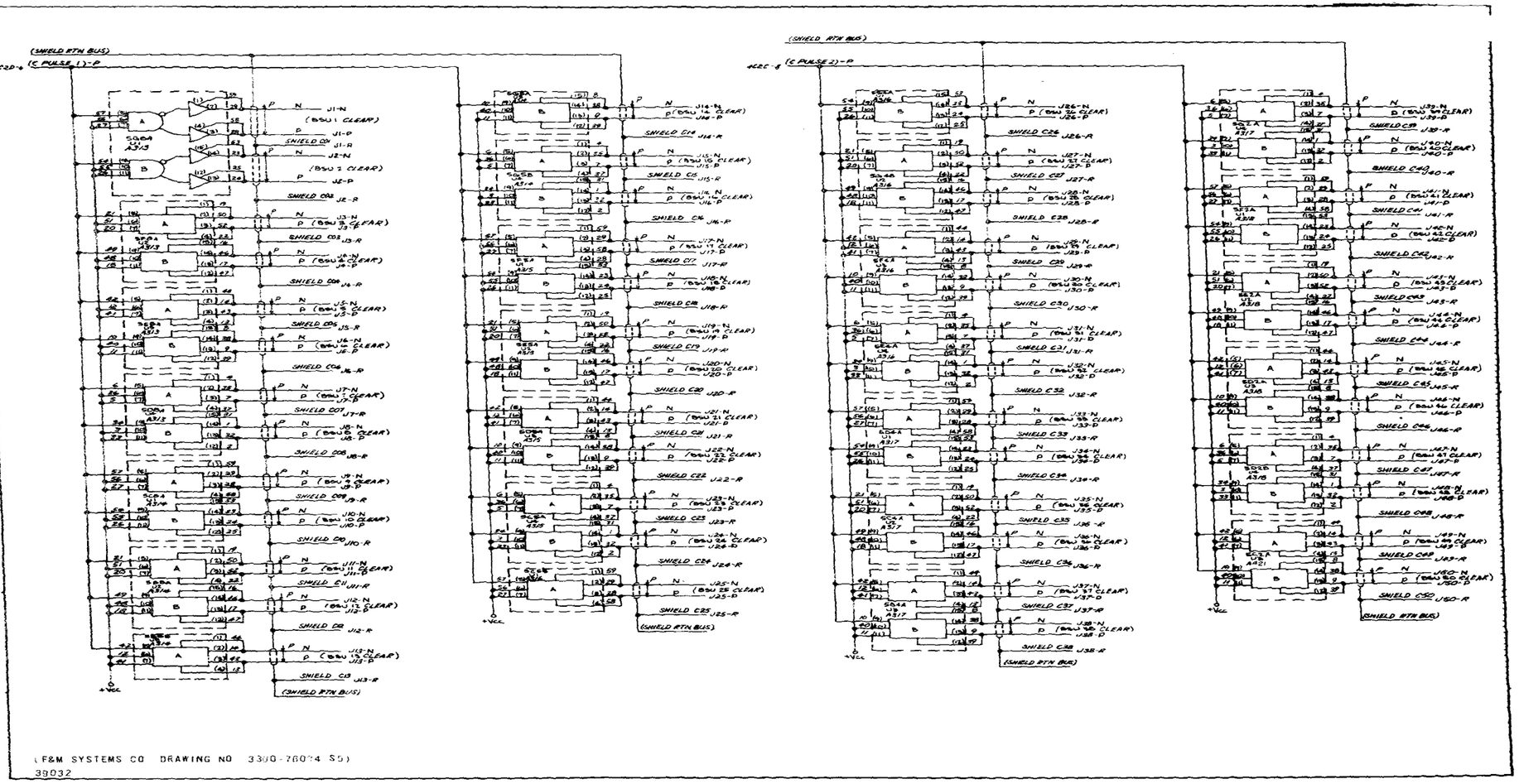


Figure 7-7. Position Scanner Logic Diagram (Sheet 5 of 20)

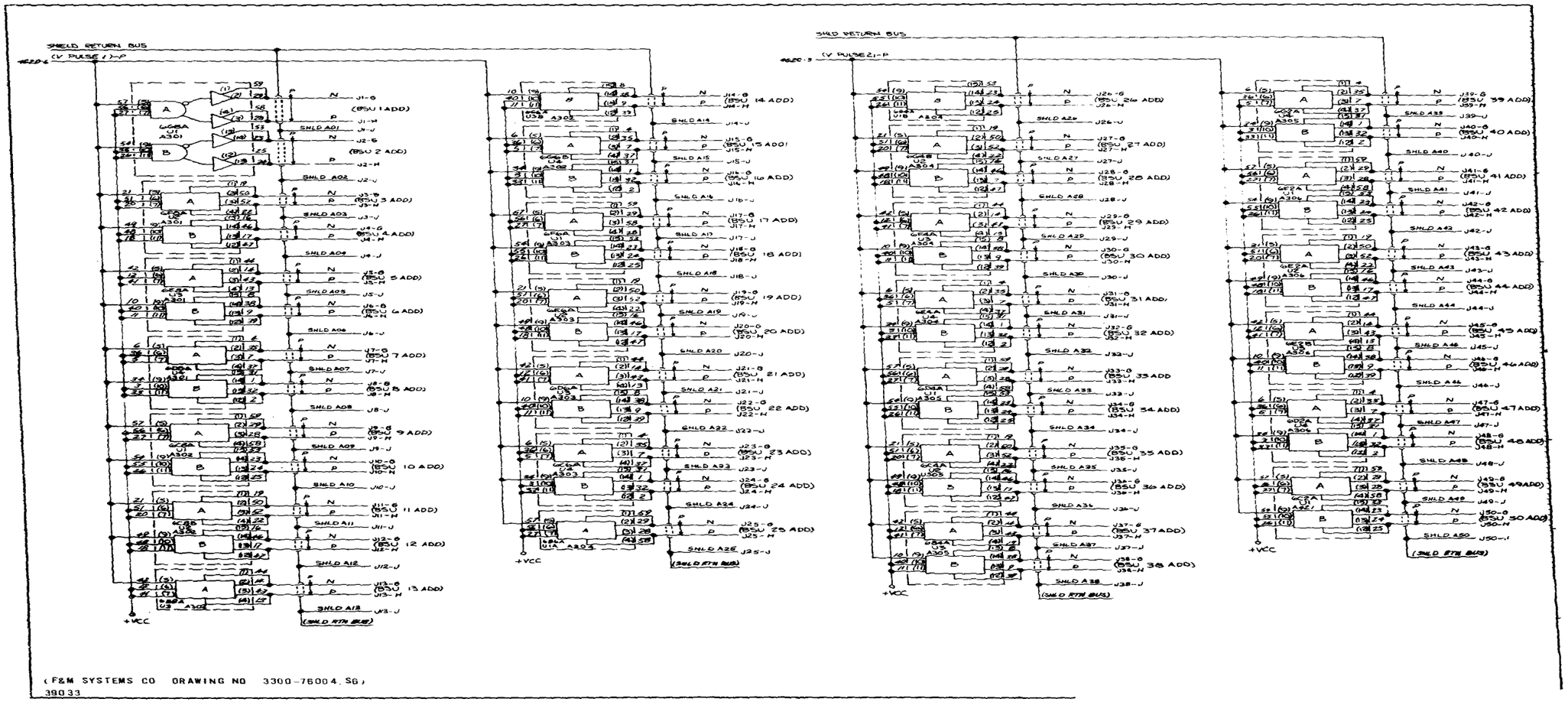
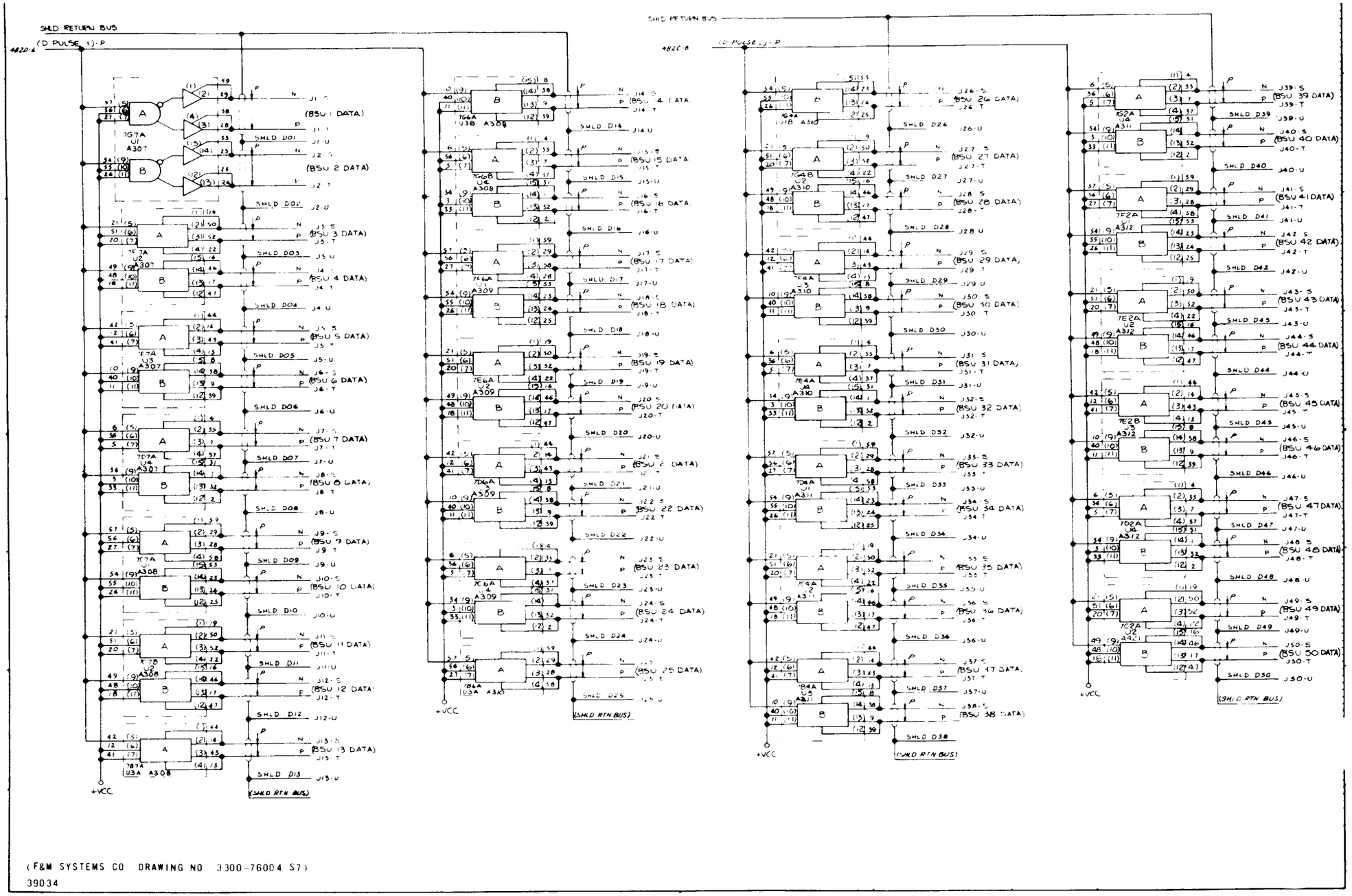


Figure 7-7. Position Scanner Logic Diagram (Sheet 6 of 20)



(F&M SYSTEMS CO DRAWING NO 3300-76004 S7)
39034

Figure 7-7. Position Scanner Logic Diagram (Sheet 7 of 20)

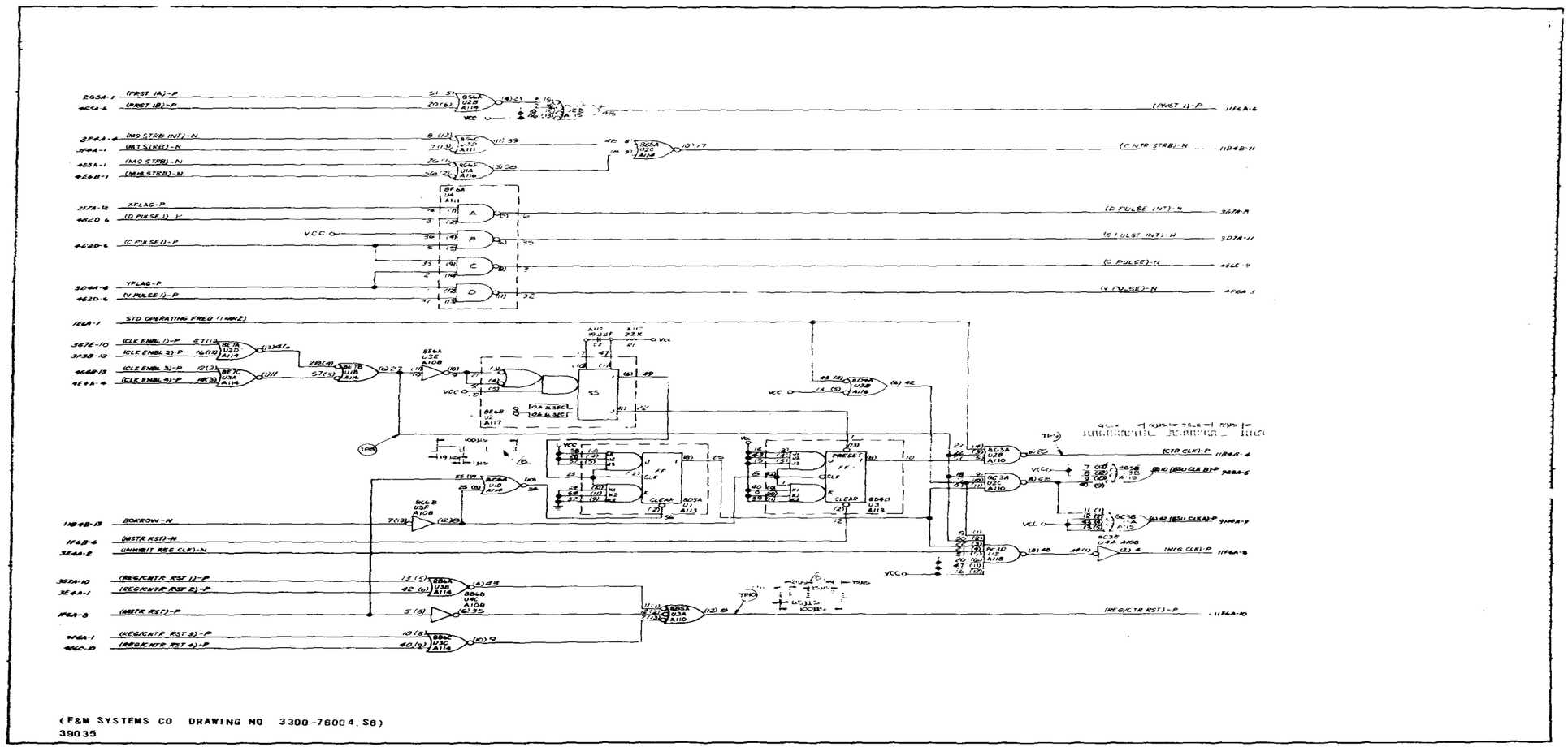
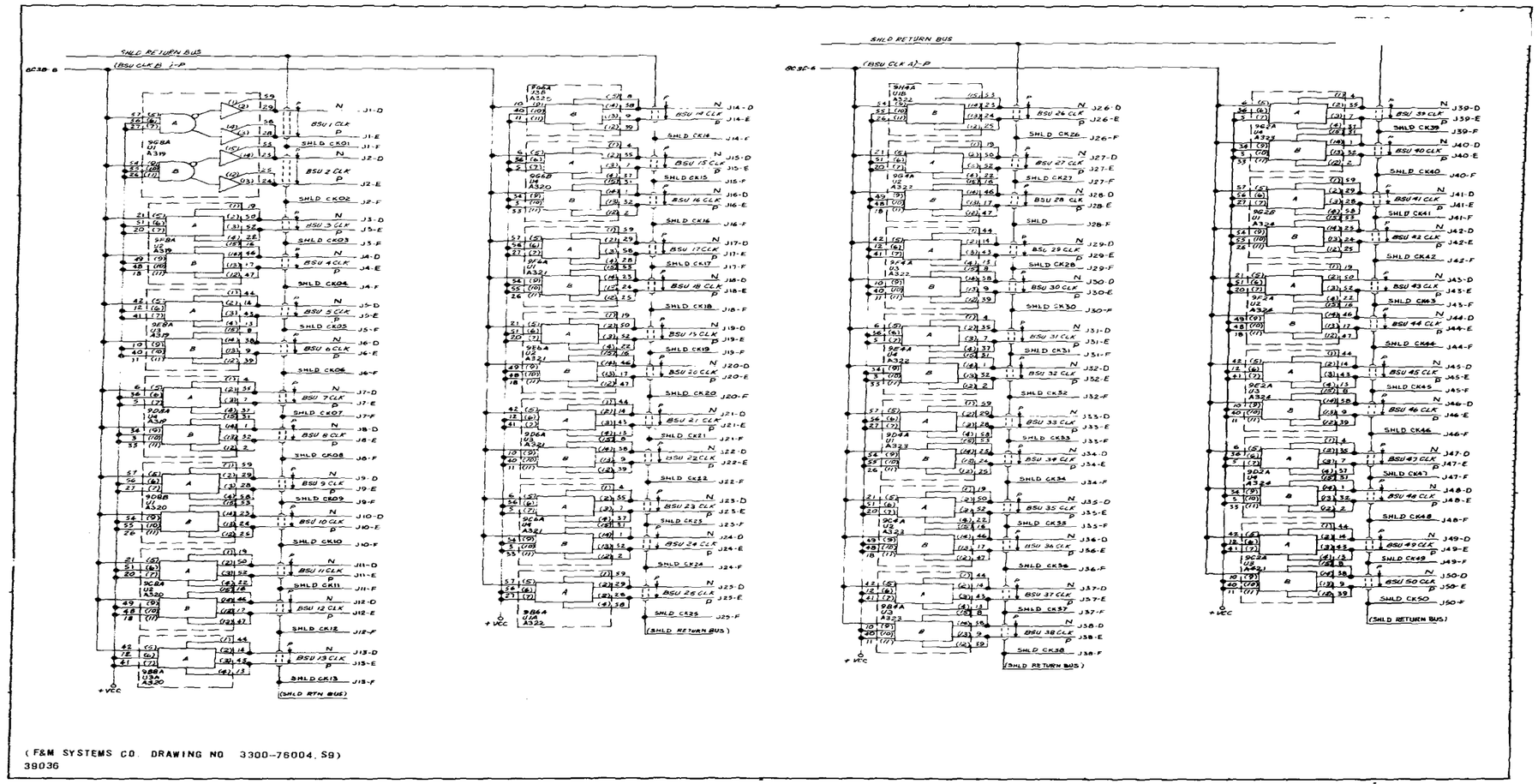


Figure 7-7. Position Scanner Logic Diagram (Sheet 8 of 20)



(F&M SYSTEMS CO. DRAWING NO. 3300-76004, S9)
38036

Figure 7-7. Position Scanner Logic Diagram (Sheet 9 of 20)

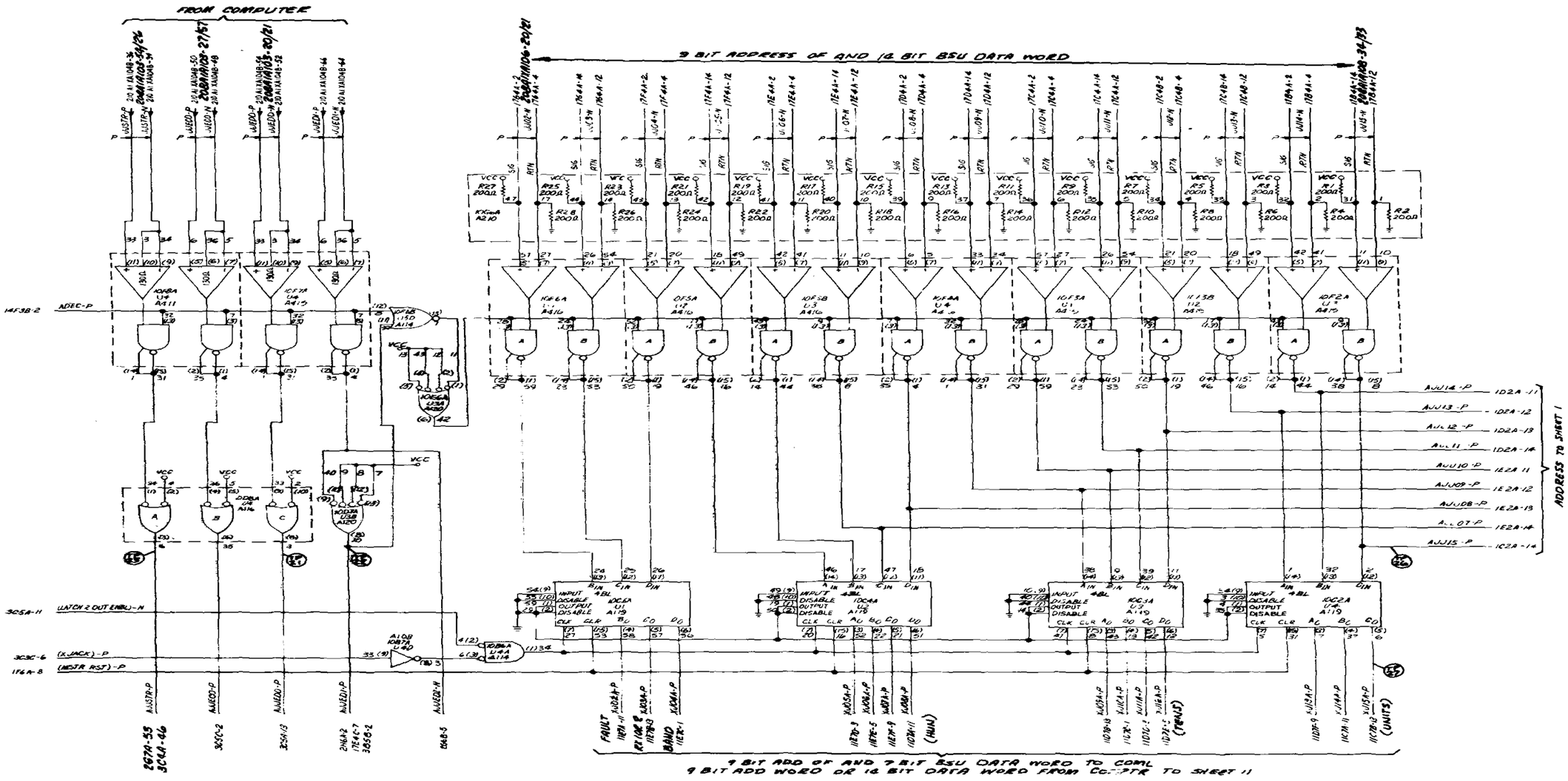


Figure 7-7. Position Scanner Logic Diagram (Sheet 10 of 20)

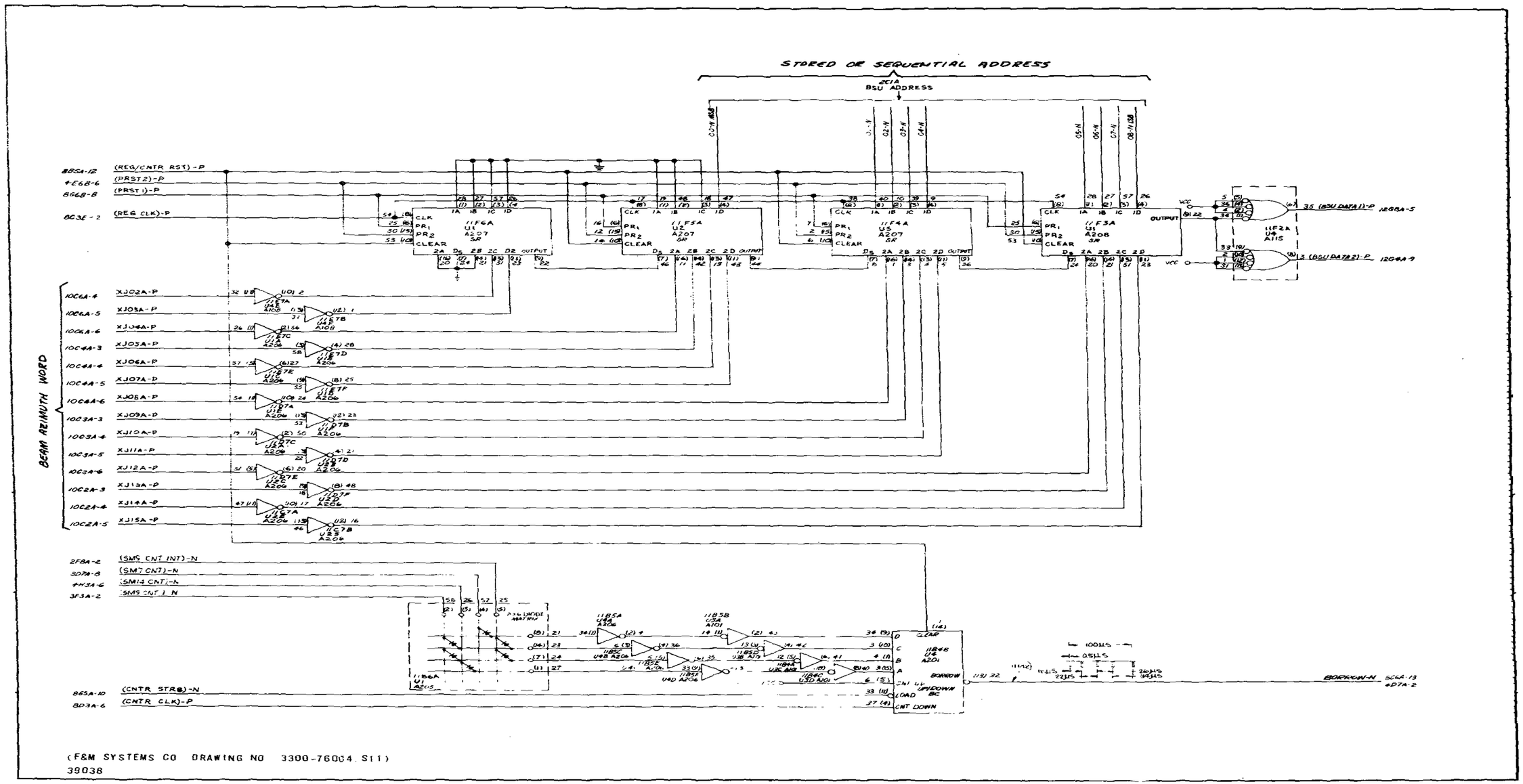
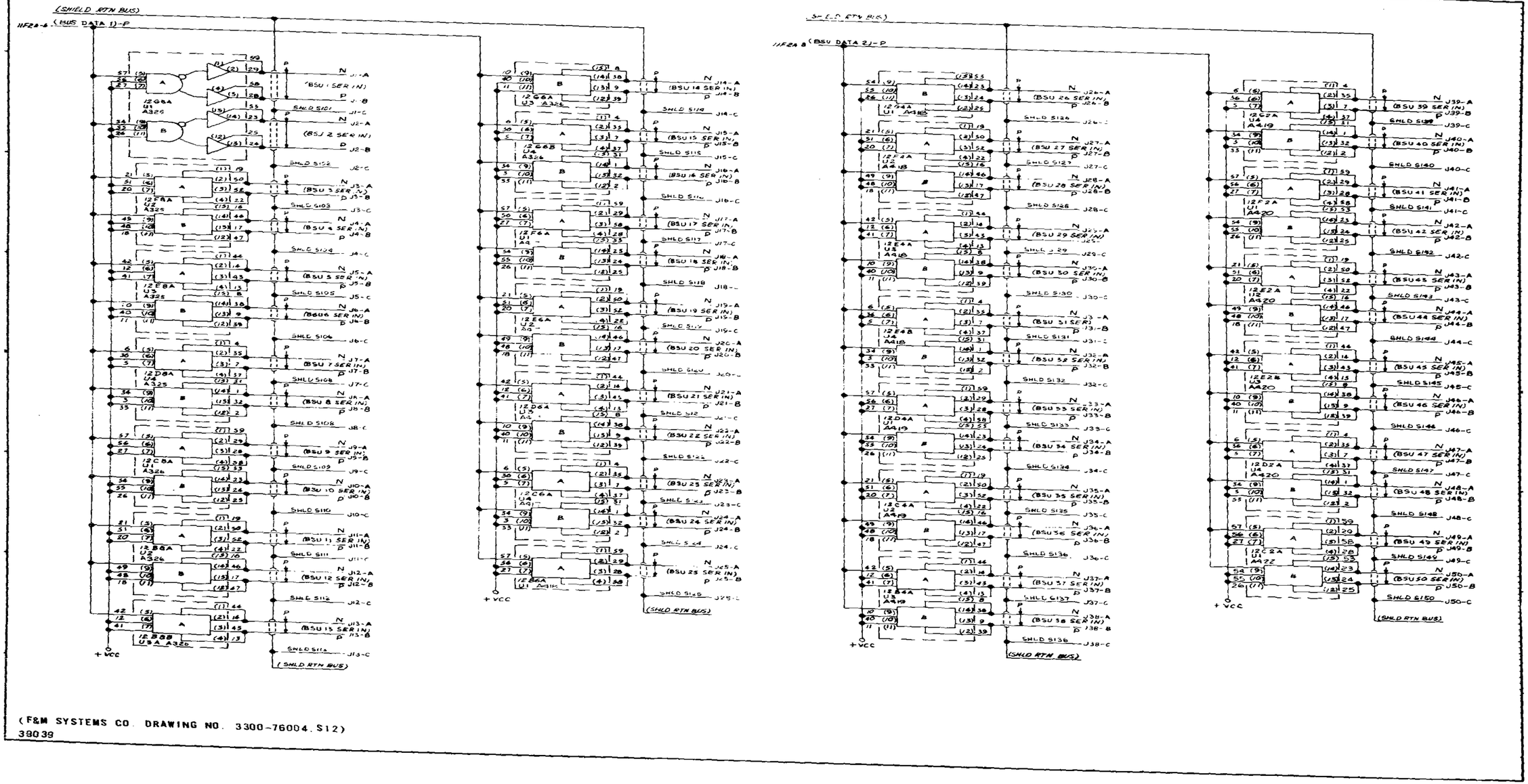


Figure 7-7. Position Scanner Logic Diagram (Sheet 11 of 20)



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39039

Figure 7-7. Position Scanner Logic Diagram (Sheet 12 of 20)

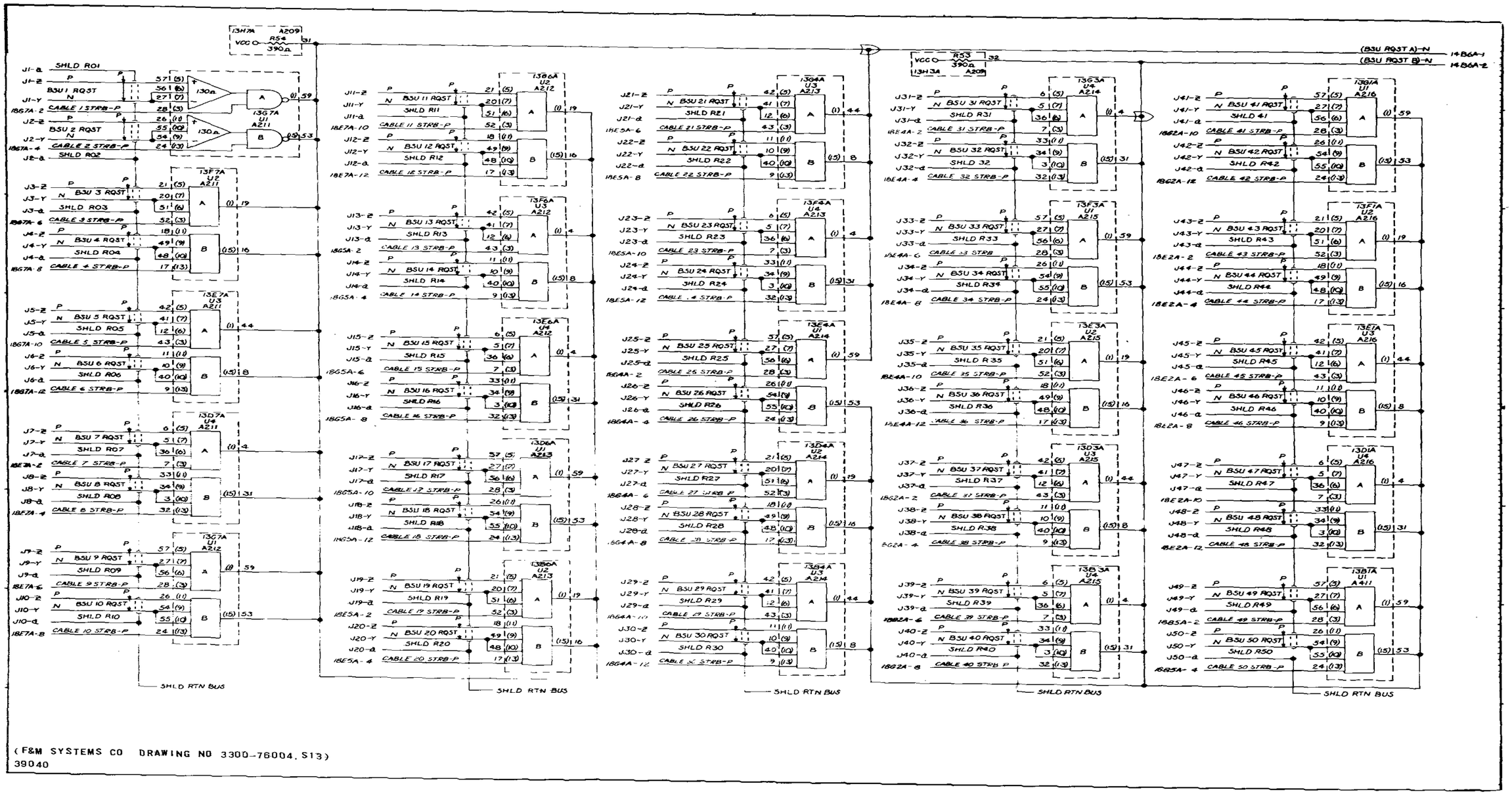
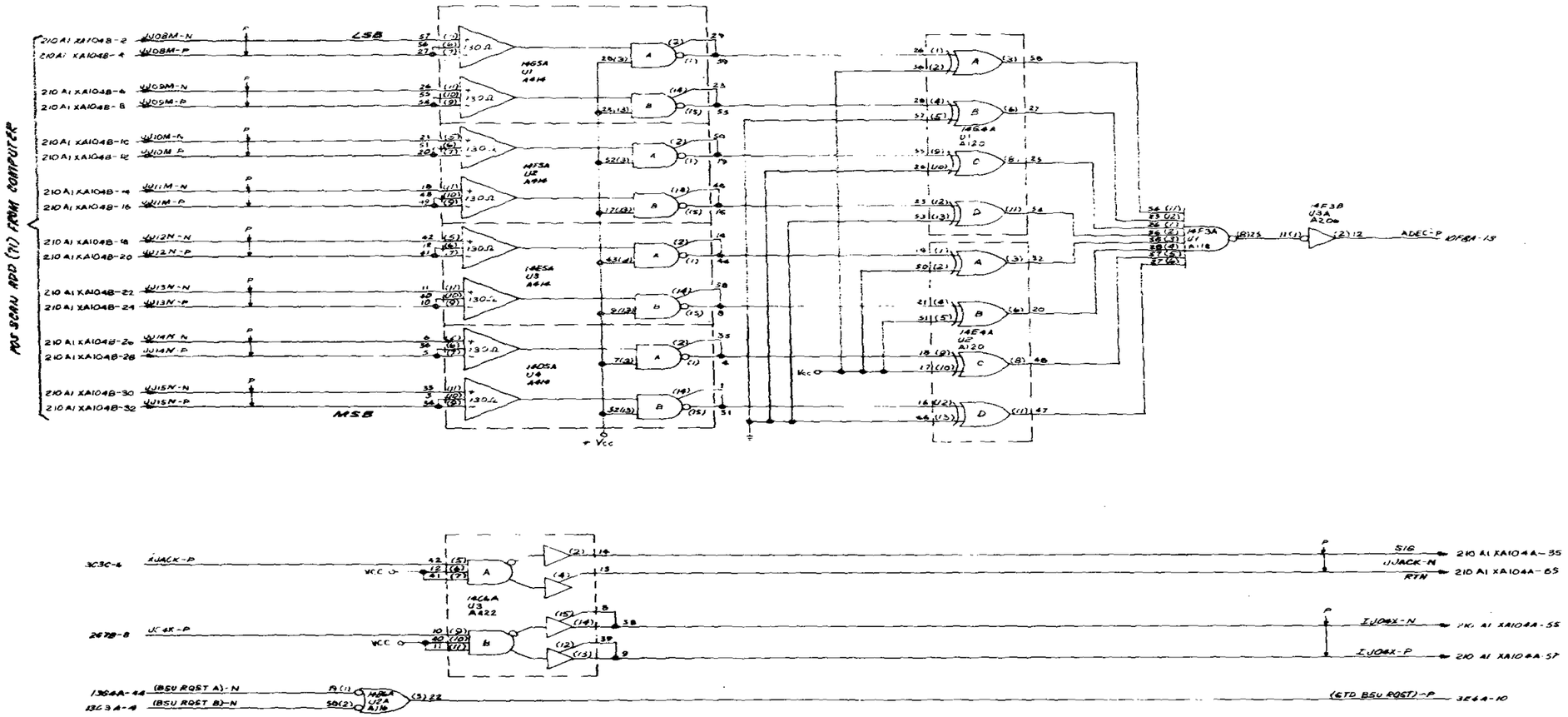


Figure 7-7. Position Scanner Logic Diagram (Sheet 13 of 20)



(F&M SYSTEMS CO DRAWING NO 3300-76004, S14)
39041

Figure 7-7. Position Scanner Logic Diagram (Sheet 14 of 20)

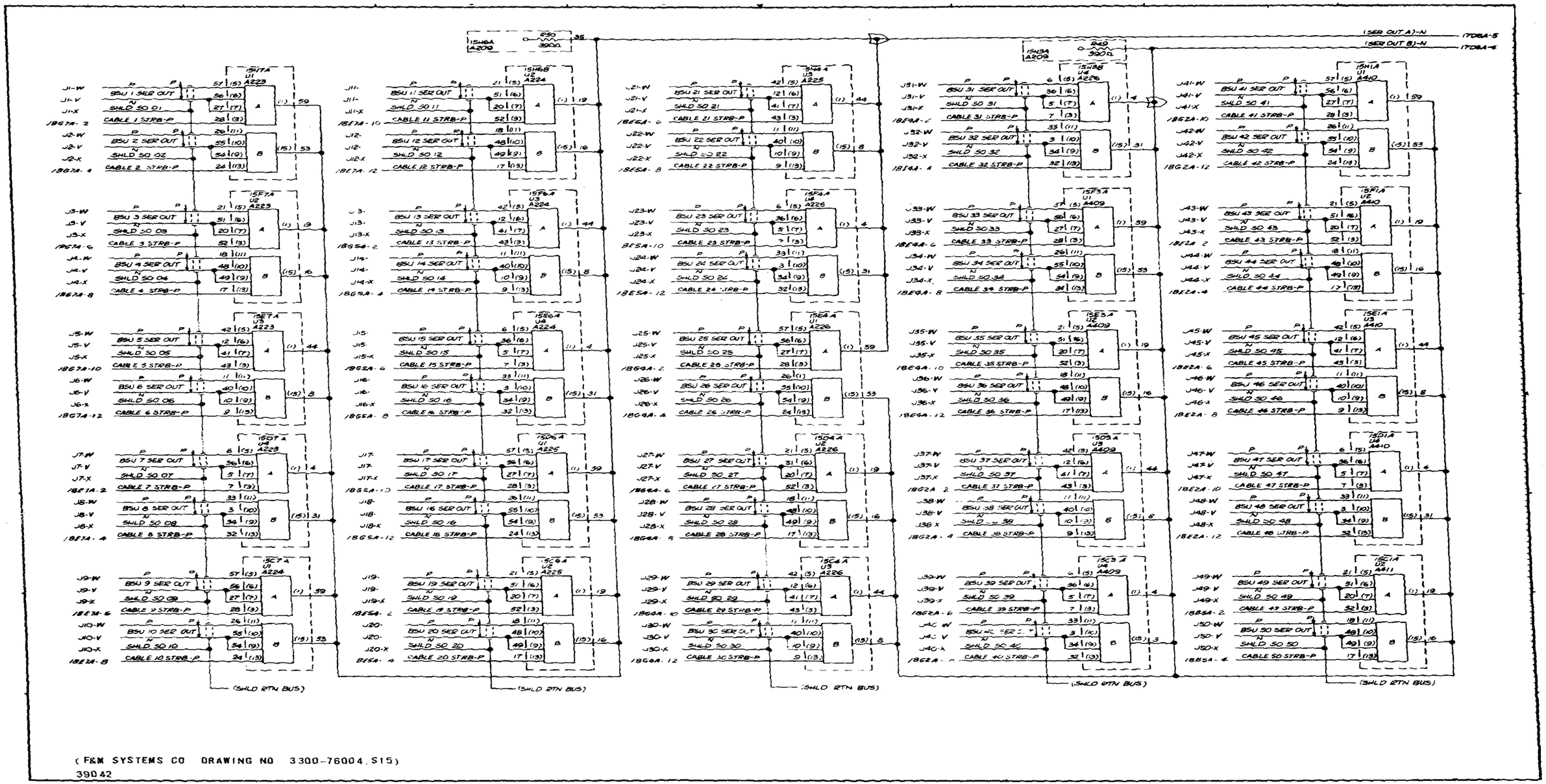


Figure 7-7. Position Scanner Logic Diagram (Sheet 15 of 20)

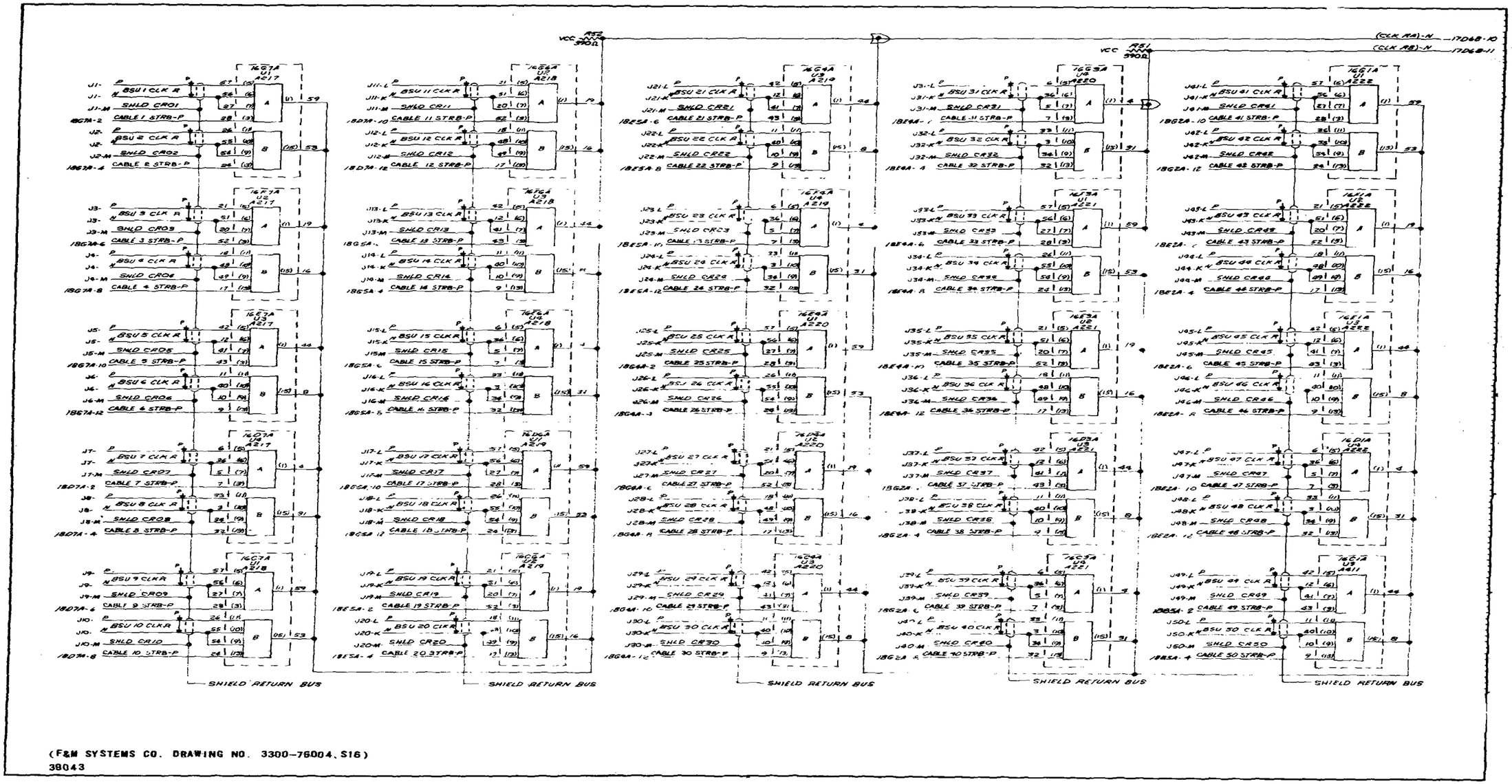
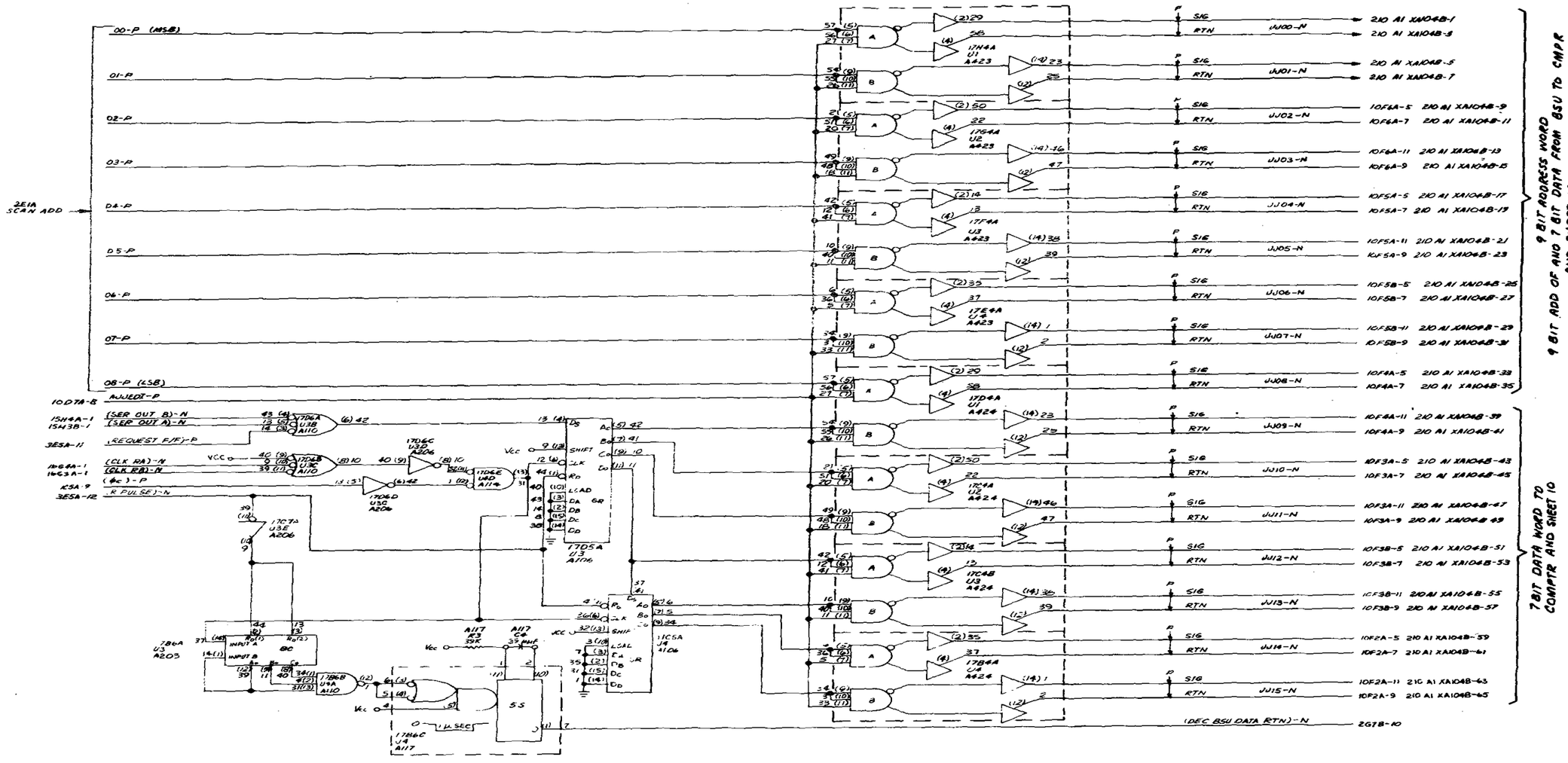
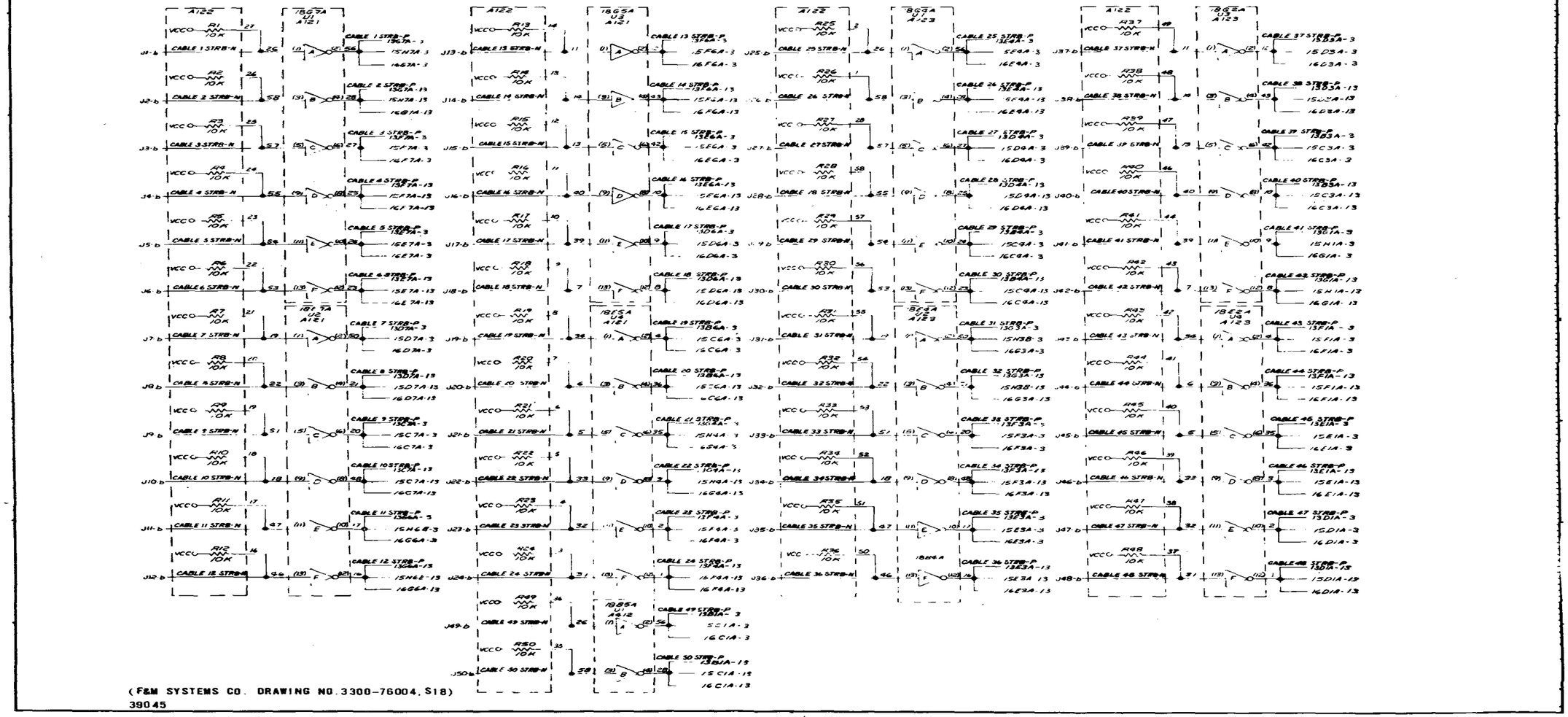


Figure 7-7. Position Scanner Logic Diagram (Sheet 16 of 20)



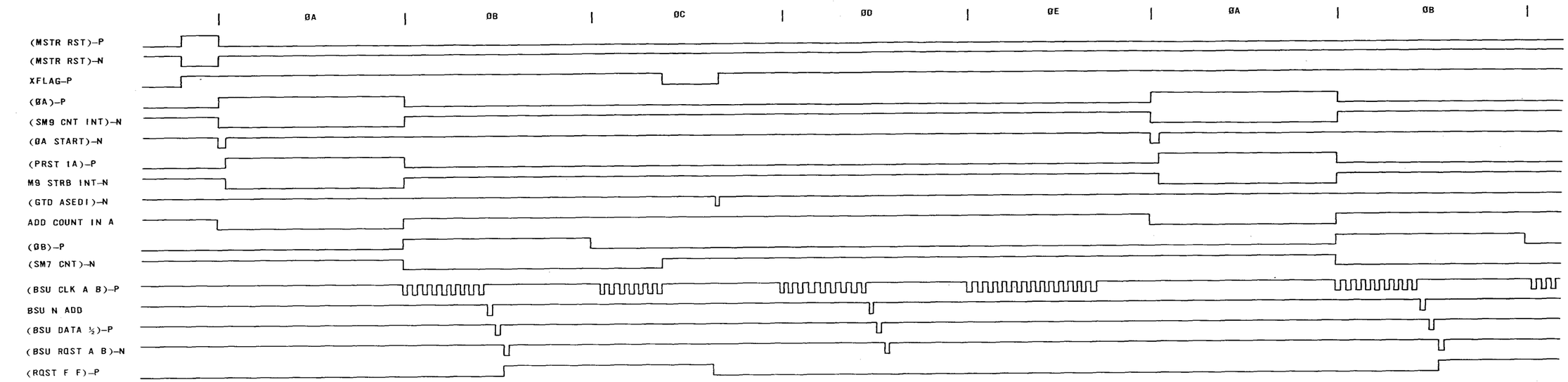
(F&M SYSTEMS CO DRAWING NO 3300-78004 S17)
39044

Figure 7-7. Position Scanner Logic Diagram (Sheet 17 of 20)



(F&M SYSTEMS CO. DRAWING NO. 3300-76004, S18)
39045

Figure 7-7. Position Scanner Logic Diagram (Sheet 18 of 20)



NOTES: 1 UNLESS OTHERWISE SPECIFIED
A. THE BASIC OPERATING FREQUENCY SHALL BE 1MHz
B. EACH CLOCK PHASE SHALL BE 20 USEC IN WIDTH
C. MODES OF OPERATION SHALL BE DEFINED AS FOLLOWS
1. INTERROGATE: PHASES A, B, AND C
2. REPLY: PHASES D AND E
D. THE INTERROGATE MODE IS ENABLED ONLY IF XFLAG IS POSITIVE TRUE (LOGICAL 1)
E. THE REPLY MODE IS ENABLED ONLY IF YFLAG IS POSITIVE TRUE (LOGICAL 1)

35938

Figure 7-7. Position Scanner Logic Diagram (Sheet 19 of 20)

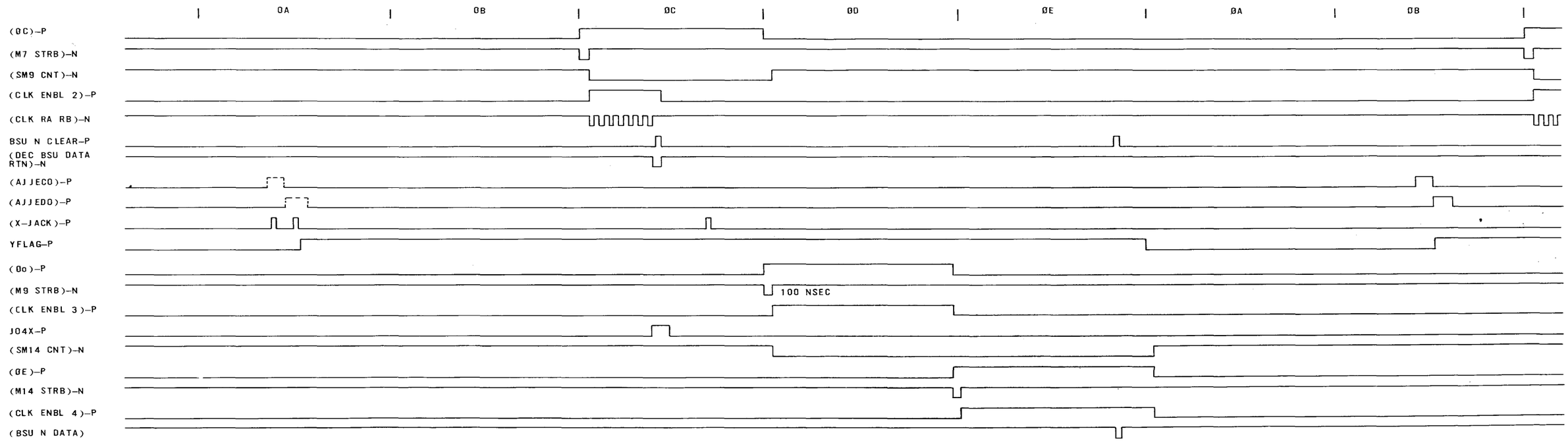
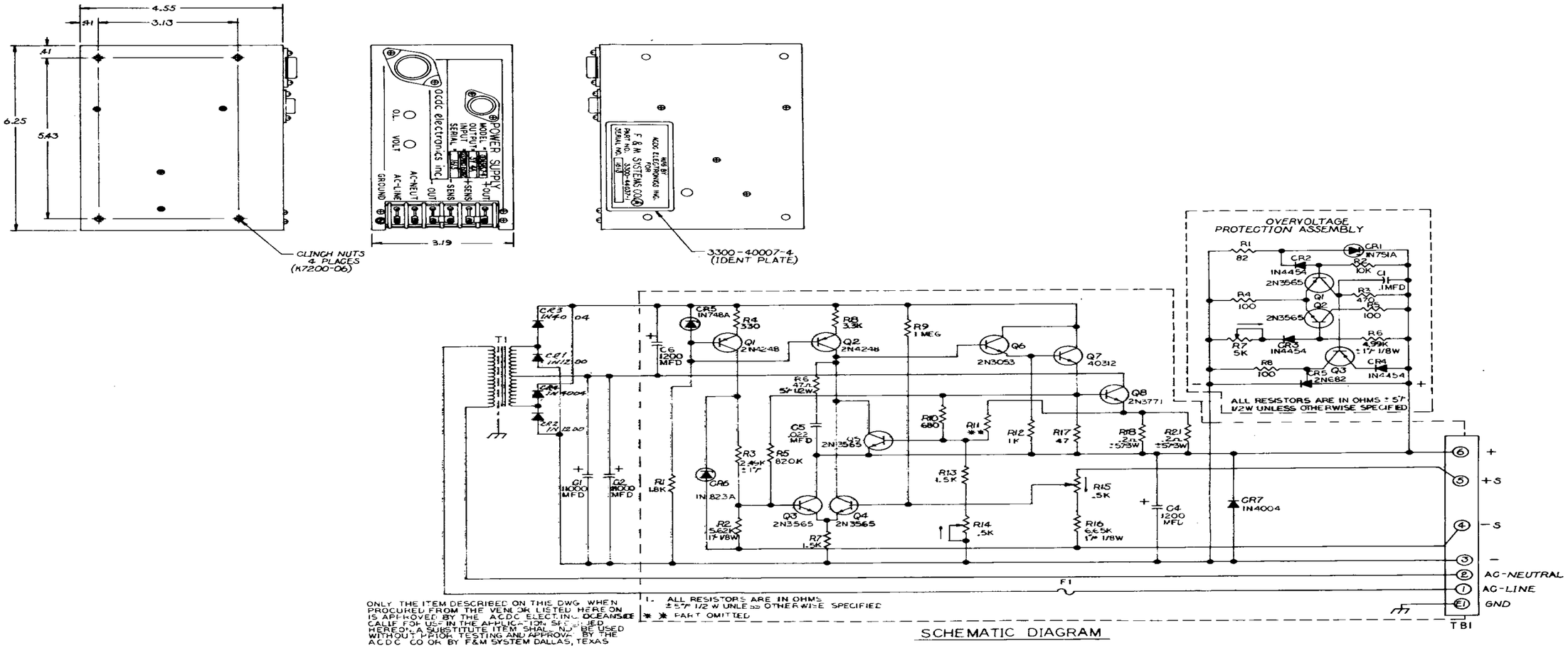


Figure 7-7. Position Scanner Logic Diagram (Sheet 20 of 20)



APPROVED SOURCE OF SUPPLY		
VENDOR	VENDOR'S ITEM IDENT NO.	APPLICATION
ACDC ELECT INC OCEANSIDE CALIF.	OEM 5N5.7-4	POWER SUPPLY

(F&M SYSTEMS CO DRAWING NO 3300-44037)
35995

Figure 7-8. Power Supply PP-6813/FLR-9(V) Schematic Diagram

By Order of the Secretary of the Army:

FRED C. WEYAND
General, United States Army
Chief of Staff

Official:

PAUL T. SMITH
Major General, United States Army
Tile Adjutant General

* U.S.GOVERMENT PRINTING OFFICE: 1976 211-340 /3300A /-3

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THE METRIC SYSTEM AND EQUIVALENTS

'NEAR MEASURE

. Centimeter = 10 Millimeters = 0.01 Meters = 0.3937 Inches
1 Meter = 100 Centimeters = 1000 Millimeters = 39.37 Inches
1 Kilometer = 1000 Meters = 0.621 Miles

'VEIGHTS

Gram = 0.001 Kilograms = 1000 Milligrams = 0.035 Ounces
1 Kilogram = 1000 Grams = 2.2 lb.
1 Metric Ton = 1000 Kilograms = 1 Megagram = 1.1 Short Tons

LIQUID MEASURE

1 Milliliter = 0.001 Liters = 0.0338 Fluid Ounces
1 Liter = 1000 Milliliters = 33.82 Fluid Ounces

SQUARE MEASURE

1 Sq. Centimeter = 100 Sq. Millimeters = 0.155 Sq. Inches
1 Sq. Meter = 10,000 Sq. Centimeters = 10.76 Sq. Feet
1 Sq. Kilometer = 1,000,000 Sq. Meters = 0.386 Sq. Miles

CUBIC MEASURE

1 Cu. Centimeter = 1000 Cu. Millimeters = 0.06 Cu. Inches
1 Cu. Meter = 1,000,000 Cu. Centimeters = 35.31 Cu. Feet

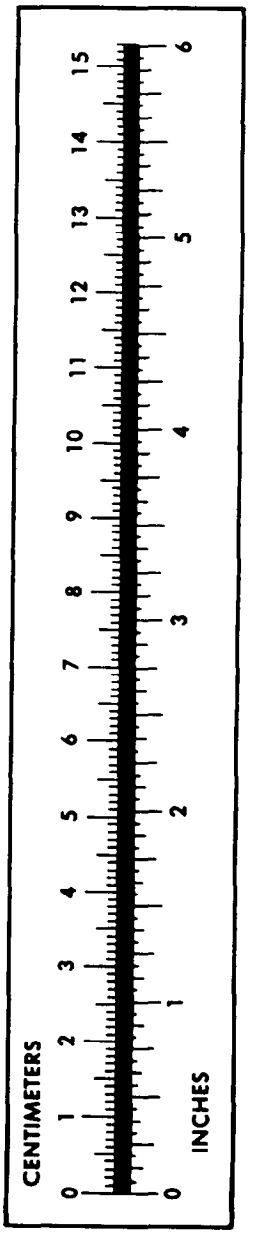
TEMPERATURE

5/9(°F - 32) = °C
212° Fahrenheit is evuivalent to 100° Celsius
90° Fahrenheit is equivalent to 32.2° Celsius
32° Fahrenheit is equivalent to 0° Celsius
9/5C° + 32 =°F

APPROXIMATE CONVERSION FACTORS

TO CHANGE	TO	MULTIPLY BY
Inches	Centimeters	2.540
Feet	Meters	0.305
Yards	Meters	0.914
Miles	Kilometers	1.609
Square Inches	Square Centimeters	6.451
Square Feet	Square Meters	0.093
Square Yards	Square Meters	0.836
Square Miles	Square Kilometers	2.590
Acres	Square Hectometers	0.405
Cubic Feet	Cubic Meters	0.028
Cubic Yards	Cubic Meters	0.765
Fluid Ounces	Milliliters	29.573
ıts	Liters	0.473
arts	Liters	0.946
allons	Liters	3.785
Ounces	Grams	28.349
Pounds	Kilograms	0.454
Short Tons	Metric Tons	0.907
Pound-Feet	Newton-Meters	1.356
Pounds per Square Inch	Kilopascals	6.895
Miles per Gallon	Kilometers per Liter	0.425
Miles per Hour	Kilometers per Hour	1.609

TO CHANGE	TO	MULTIPLY BY
Centimeters	Inches	0.394
Meters	Feet	3.280
Meters	Yards	1.094
Kilometers	Miles	0.621
Square Centimeters	Square Inches	0.155
Square Meters	Square Feet	10.764
Square Meters	Square Yards	1.196
Square Kilometers	Square Miles	0.386
Square Hectometers	Acres	2.471
Cubic Meters	Cubic Feet	35.315
Cubic Meters	Cubic Yards	1.308
Milliliters	Fluid Ounces	0.034
Liters	Pints	2.113
Liters	Quarts	1.057
ers	Gallons	0.264
ms	Ounces	0.035
ograms	Pounds	2.205
Metric Tons	Short Tons	1.102
Newton-Meters	Pounds-Feet	0.738
Kilopascals	Pounds per Square Inch	0.145
lometers per Liter	Miles per Gallon	2.354
meters per Hour	Miles per Hour	0.621



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